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SiC Discrete Power Devices

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13. ABSTRACT (Maximum 200 words)

A first order analysis was performed to determine the voltage-ratings upto which 4H-SiC, 6H-SiC unipolar devices (FETs) have lower forward voltage drops than silicon, 4H-SiC, 6H-SiC bipolar devices (IGBTs). It was found that 4H-SiC unipolar devices have the lowest forward voltage drops upto a voltage-rating of 4500V. The problems associated with a SiC power MOSFET are presented and alternatives to the power MOSFET, the JFET and the U-MESFET are discussed. Two dimensional simulations using MEDICI were performed to analyze the performance of a 1000V 4H-SiC U-MESFET. The U-MESFET was found to be an excellent device, with a low specific on-resistance close to the ideal value.

The fabrication of a U-MESFET involves filling deep trenches with metal which is complicated. Further, when a metal gate is used, it is difficult to achieve gate to source isolation. A novel trench-gate heterojunction FET (HJFET) structure was analyzed to surpass this problem. The fabrication of the HJFET involves a six mask level process with no critical alignments. A process sequence for the fabrication of the HJFET was developed. The problems encountered during the fabrication and proposed solutions are outlined. Results of the experimental measurements on the fabricated HJFET are presented.

A system has been fabricated for the chemical vapor deposition of 4H- and 6H-SiC thin films. The unique design incorporates a separate load lock from which the growth chamber and a reflection high energy electron diffraction (RHEED) chamber are attached. Most of the system hardware has been assembled. Electrical wiring and gas line assembly has been completed to the extent possible. All power supply components have been received. Recently implemented safety concerns have resulted in the current retrofitting of newly assigned laboratory space to address these issues.

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I. Introduction

At present, semiconductor power devices are commonly used to control heavy machinery and equipment. The principal semiconductor from which these power devices are manufactured is silicon. For many applications, the power MOSFET is the commonly used device. In order to minimize the power losses in the power MOSFET, it is necessary to reduce the on-resistance of the device. Progress in silicon power technology has been successful in pushing the on-resistance of the MOSFET close to the theoretical limits [1,2]. It is therefore necessary to consider other semiconductor materials if further improvements in device performance need to be attained. Silicon Carbide (SiC) is one such semiconductor.

Due to the high critical electric field for breakdown in SiC (compared to silicon) a power device with a given voltage rating can be fabricated using a drift-region whose doping is much higher than that in silicon [3]. Hence the on-resistance in SiC power devices will be much lower than that in silicon power devices, for the same voltage-rating. In 1983 Baliga [4] derived a figure of merit

$$BFOM = \varepsilon \mu E_G^3 \qquad (1)$$

which defines material parameters to minimize conduction losses in power FETs. Here ε is the dielectric constant, μ is the mobility and E_G is the band-gap of the semiconductor. Table 1 gives some of the electrical and material parameters of Si, 6H-SiC, 4H-SiC and diamond for power device applications [3,5-7]. From these values and equation 1 it can be seen that FETs made using SiC and diamond will have lower on-state losses than silicon FETs. Good quality epitaxial layers of 6H-SiC and 4H-SiC are commercially available at present. The FET structures on these materials need to be investigated. This is the aim of the present work.

Property	Silicon	6H-SiC	4H-SiC	Diamond
Band-gap (eV)	1.1	2.86	3.2	5.5
electron mobility (cm^2/V-s)	1400	84*	1140*	1870
hole mobility (cm^2/V-s)	600	99	108	250
break down electric field	$3x10^5$V/cm	$5x10^6$V/cm	$5x10^6$V/cm	$7x10^6$V/cm
dielectric constant	11.8	9.7	9.7	11.9

*these values are for mobility along the c-axis.

Table 1 : Material parameters for silicon, silicon carbide and diamond.

The contents of the sections to follow are briefly described in the following paragraphs. A first order analysis, to determine the voltage-ratings up to which unipolar devices have lower forward voltage drop than bipolar devices, is performed in section **II**. The forward voltage drops of 4H-SiC unipolar devices are compared to the forward voltage drops of silicon bipolar devices for voltage-ratings ranging from 500 V - 40,000 V

at different temperatures of operation. Similar analysis is performed for 6H-SiC unipolar and silicon bipolar devices, 4H-SiC unipolar and 4H-SiC unipolar devices and 6H-SiC unipolar and 6H-SiC bipolar devices.

In section **III**, problems associated with the operation of a SiC MOSFET and alternatives to the MOSFET are considered. The performance of a 1000 V 4H-SiC U-MESFET was studied using numerical simulations and the results are presented. Problems associated in fabricating the U-MESFET structure are discussed.

In section **IV**, a novel trench-gate heterojunction FET (HJFET) structure, with a six mask level process sequence for fabrication, is analyzed. A process sequence for fabrication of 4H-SiC and 6H-SiC HJFETs and the problems encountered during the fabrication are discussed in detail.

Section **V** deals with the experimental measurements on the fabricated HJFET. The results of the experimental measurements are discussed and suggestions for future work on the HJFET are outlined. Each section is self contained with its own figures, tables and references.

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II. First Order Analysis of Unipolar Versus Bipolar SiC Devices

A. Introduction

Silicon Carbide (SiC) has been shown to be an excellent semiconductor for the development of high voltage, high temperature and high frequency devices. The intrinsic carrier concentration in SiC is extremely low due to its large band gap compared to silicon. This enables devices fabricated from SiC to be operated at a much higher temperature than devices fabricated from silicon. Also SiC has a high critical electric field for breakdown compared to silicon. This allows the use of much higher doping and thinner epi-layers for a given breakdown voltage than is required in Si devices, resulting in much lower specific on-resistances for unipolar power devices [1].

Power devices can be broadly classified into unipolar and bipolar devices. In unipolar devices the on-state voltage drop is determined by the resistance of the drift region. The forward conduction losses are therefore determined by the drift region doping and thickness and hence increase with the voltage rating of the device. The power MOSFET is a commonly used unipolar device. In bipolar devices, on-state conduction occurs by injection of carriers across a p-n junction resulting in conductivity modulation of the drift-region. Consequently, the on-state voltage drop is determined by the contact potential of the p-n junction, because the voltage drop across the drift-region becomes small. The IGBT is the most commonly used high voltage MOS gated bipolar device. In case of the IGBT, assuming minority carrier life-times are high, the forward conduction losses are largely determined by the contact potential (V_{bi}) of the p-n junction and remain fairly constant over a large range of breakdown voltage ratings.

B. Objective of the first order analysis

For relatively small voltage ratings, thin epi-layers with high doping are needed and the voltage drop across the drift region is much lower than the contact potential. Hence it is advantageous to use unipolar devices for these applications. For higher voltage ratings, thicker low doped layers are used and the drift region drop becomes large compared to the contact potential. In bipolar devices, there is conductivity modulation of the drift-region, due to injection of minority carriers across the p-n junction, this results in a nearly constant forward voltage drop independent of the drift-region doping or thickness. Hence bipolar devices have lower on-state voltage drops than unipolar devices at high voltage ratings.

For unipolar devices, taking into account only the drift-region resistance the forward voltage drop can is given by:

$$V = \frac{JW_{C,PP}}{q\mu_n N} \qquad (1)$$

where J is the current density in the on-state, q is the electron charge, N is the doping of the material, μ_n is the electron mobility, $W_{C,pp}$ is the drift-region width [2]. The electron

mobility decreases as the temperature of operation increases: $\mu_n \alpha (T/300)^{-2.42}$ for silicon and $\mu_n \alpha (T/300)^{-1.8}$ for SiC [2,3]. Hence, the forward voltage drop for a unipolar device increases with increase in temperature. In bipolar devices, since V_{bi} decreases with temperature, the forward voltage drop actually decreases with temperature. Thus unipolar devices are suitable for low voltage and low temperature applications and bipolar devices are better suited for higher voltages and temperatures.

In general, unipolar devices are preferred over bipolar devices, due to their superior switching characteristics and safe-operating area (SOA) [2]. For silicon power devices, unipolar devices (power MOSFETs) are used for voltage ratings up to 200 V and bipolar devices are used for higher voltage ratings, in order to keep the on-state losses to a minimum. For a given voltage rating, SiC unipolar devices have a much lower specific on-resistance (about 200 times lesser) than silicon unipolar devices [1]. Hence, SiC unipolar devices can be used for much higher voltage ratings than Si unipolar devices. The forward voltage drop in bipolar devices depends on the band-gap of the material (increases with increasing band gap) and is fairly independent of the voltage rating of the device due to conductivity modulation of the drift-region. Hence, silicon (E_g = 1.1 eV) bipolar devices will always have a lower forward voltage drop than 6H-SiC (E_g = 2.86 eV) or 4H-SiC (E_g = 3.2 eV) bipolar devices. Typical on-state J-V characteristics for silicon, 6H-SiC, 4H-SiC IGBTs are shown in figure 1. Silicon has the lowest band-gap and hence silicon IGBTs have lower forward voltage drops than 6H-SiC or 4H-SiC IGBTs. The objective of this analysis is to determine the voltage rating above which the forward voltage drop of SiC unipolar devices exceeds that of silicon bipolar devices and SiC bipolar devices.

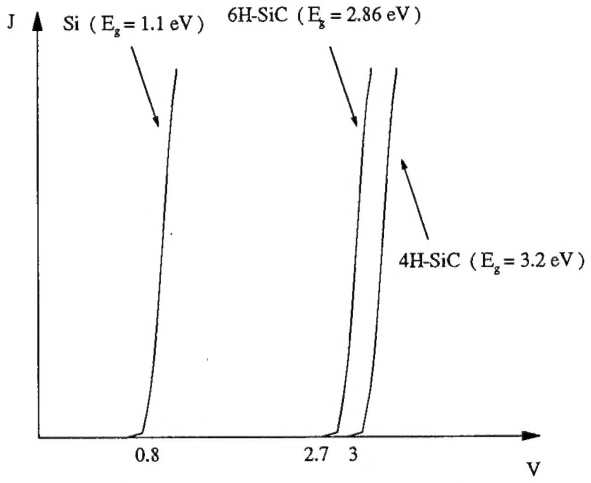

Fig.1 : Typical Forward J-V characteristics for Si, 6H-SiC, 4H-SiC IGBTs, the forward voltage drop for the silicon IGBT is the lowest.

C. Analysis

For a simple first order analysis, the forward voltage drop of a unipolar device can be assumed to be the same as the drift-region voltage drop and the forward voltage drop is given by equation 1.

The forward voltage drop of a bipolar device can be assumed to be the same as that for a P-I-N rectifier and the forward voltage drop is given by:

$$V = \frac{2kT}{q} \ln\left(\frac{Jd}{2qD_a n_i F(d / L_a)}\right) \qquad (2)$$

where n_i is the intrinsic carrier concentration, D_a is the ambipolar diffusion coefficient, L_a is the ambipolar diffusion length and d is $W_{C,PP}/2$. For this analysis, it is assumed that the minority carrier lifetimes are high enough such that $L_a = d$, i.e. $F(d / L_a)$ has its maximum value of 0.3 [2].

C.1. Analysis of cross-over current density

Figure 2 shows the typical forward J-V characteristics of a unipolar and bipolar device at two different voltage ratings. The current density at the point at which the two curves intersect will be defined as cross-over current density (J_C). J_C depends on the voltage rating of the device. As the voltage rating of the device increases, the drift-region doping decreases. This results in an increase in the forward voltage drop for unipolar devices. In case of bipolar devices, due to conductivity modulation of the drift-region the increase in forward voltage drop is much smaller. Thus, the J-V curves for unipolar and bipolar devices intersect at a lower value of current density as the voltage-rating of the device increases, as illustrated in figure 2 (i.e. $J_{C2} < J_{C1}$). For a given voltage rating, if the operating current density in the on-state is greater than J_C then a bipolar device will have a lower on-state voltage drop. If a device needs to be operated at a current density below J_C at a given voltage-rating then a unipolar device is preferred.

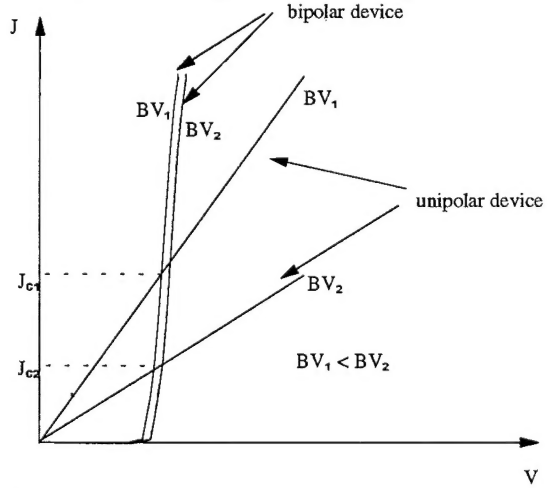

Fig. 2 : Typical Forward J-V characteristics for unipolar and bipolar devices showing the cross-over current density (J_C). J_C decreases as the breakdown voltage of the device increases.

For a given breakdown voltage rating (BV_{PP}) and temperature (T), the value of J_C can be extracted from equations (1) and (2) by equating their right hand sides and solving for J_C. The variations of N, $W_{C,pp}$ with the breakdown voltage (BV_{PP}) for SiC and silicon are given in table-1 [4-6]. The variation of the mobility with doping and temperature are also given in this table. Using these relations, J_C was calculated for 4H-SiC unipolar devices and silicon bipolar devices for voltage ratings varying from 500 V to 40000 V and temperatures of 300 K, 400 K and 500 K. Figure 3 shows the plot of J_C versus BV_{PP} for 4H-SiC unipolar and silicon bipolar devices for 3 different temperatures of operation. Figure 4 shows a similar plot for 6H-SiC unipolar and silicon bipolar devices. Plots comparing 4H-SiC unipolar devices to 4H-SiC bipolar devices and 6H-SiC unipolar devices to 6H-SiC bipolar devices are shown in figures 5 and 6, respectively. At a given temperature, J_C is a function of BV_{PP}, the variation of J_C with BV_{PP} can be determined from the curves shown in these figures or by using the relations given in table 2.

The analysis indicates that the cross-over current density for 4H-SiC unipolar and silicon bipolar devices reaches 100 A / cm^2 at approximately 4500 V at 300 K. Thus for room temperature operation, if the operating current density $\leq$ 100 A / cm^2, 4H-SiC unipolar devices will have a lower forward voltage drop than silicon bipolar devices for voltage-ratings up to 4500 V. The cross-over current density for 4H-SiC unipolar and 4H-SiC bipolar devices reaches 100 A / cm^2 at approximately 7000 V at 300 K. Thus for room temperature operation, for current densities $\leq$ 100 A / cm^2 , 4H-SiC unipolar devices will have a lower forward voltage drop than 4H-SiC bipolar devices for voltage-ratings up to 7000 V.

	silicon	4H-SiC	6H-SiC
Band-gap (E_g)	1.1 eV	3.2 eV	2.86 eV
n_i (at 300 K)	1.4×10^{10}	1.1×10^{-8}	7.6×10^{-6}

Table 1 (a)

Silicon

Doping : $N = 2 \times 10^{18} (BV_{PP})^{-4/3}$

Depletion Width at break down : $W_{C,PP} = 2.58 \times 10^{-6} (BV_{PP})^{7/6}$

Electron Mobility : $$\mu_n = \frac{5.10 \times 10^{18} + 92\, N^{0.91}}{3.75 \times 10^{15} + N^{0.91}} \left(\frac{T}{300}\right)^{-2.42}$$

Hole Mobility : $$\mu_p = \frac{2.90 \times 10^{15} + 47.7\, N^{0.76}}{5.86 \times 10^{12} + N^{0.76}} \left(\frac{T}{300}\right)^{-2.2} \qquad [2]$$

Table 1 (b)

4H-SiC

Doping : $N = 2.265 \times 10^{20} (BV_{PP})^{-1.355}$

Depletion Width at break down : $W_{C,PP} = 2.1766 \times 10^{-7} (BV_{PP})^{-1.1775}$

Electron Mobility : $$\mu_n = \frac{1140}{1+\left(\frac{N}{1.94 \times 10^{17}}\right)^{0.61}} \left(\frac{T}{300}\right)^{-1.8}$$

Hole Mobility : $$\mu_p = 15.9 + \frac{108}{1+\left(\frac{N}{1.76 \times 10^{19}}\right)^{0.34}} \left(\frac{T}{300}\right)^{-1.8}$$ [3, 4]

Table 1 (c)

6H-SiC

Doping : $N = 2.265 \times 10^{20} (BV_{PP})^{-1.355}$

Depletion Width at break down : $W_{C,PP} = 2.1766 \times 10^{-7} (BV_{PP})^{-1.1775}$

Electron Mobility : $$\mu_n = \frac{86.46}{1+\left(\frac{N}{1.11 \times 10^{18}}\right)^{0.59}} \left(\frac{T}{300}\right)^{-1.8}$$

Hole Mobility : $$\mu_p = 6.8 + \frac{92.2}{1+\left(\frac{N}{2.1 \times 10^{19}}\right)^{0.31}} \left(\frac{T}{300}\right)^{-1.8}$$ [3, 4]

Table 1 (d)

Table 1 (a-d): Material constants used in the First Order Analysis

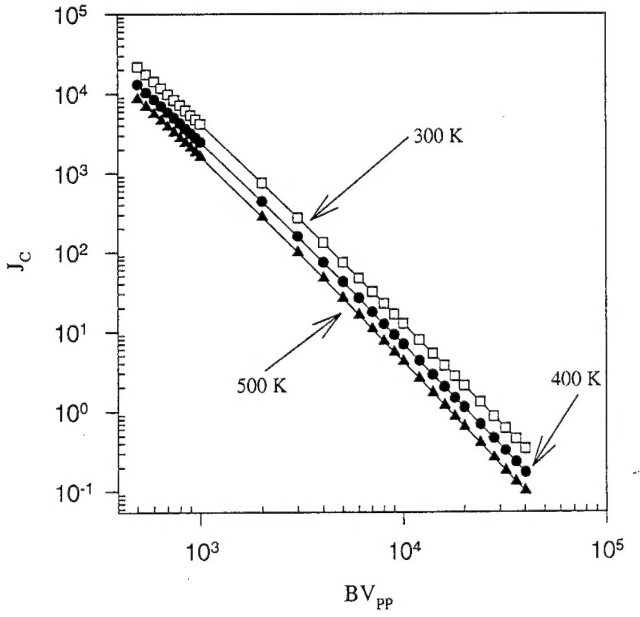

Fig. 3 : Variation of cross-over current density for 4H-SiC unipolar and Si bipolar devices with voltage-rating and temperature of operation.

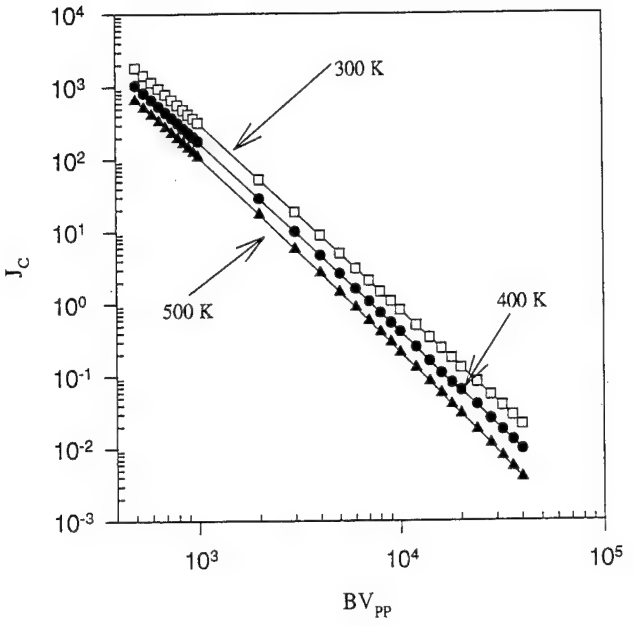

Fig. 4 : Variation of cross-over current density for 6H-SiC unipolar and Si bipolar. devices with voltage-rating and temperature of operation.

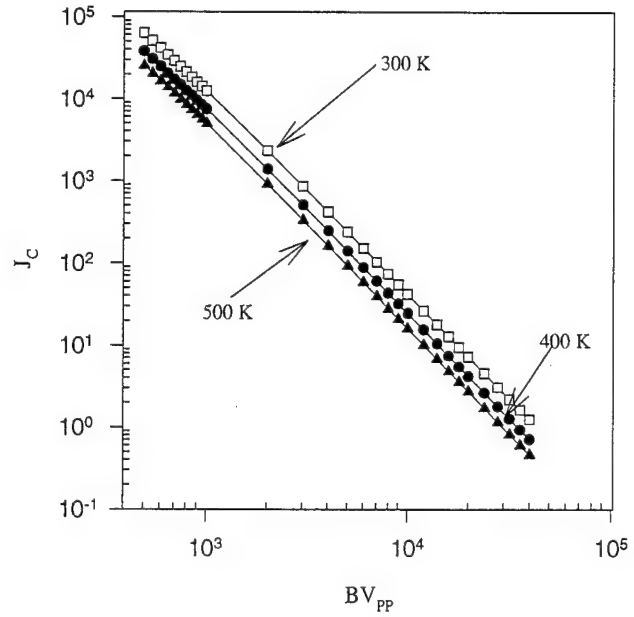

Fig. 5 : Variation of cross-over current density for 4H-SiC unipolar and bipolar devices with voltage-rating and temperature of operation..

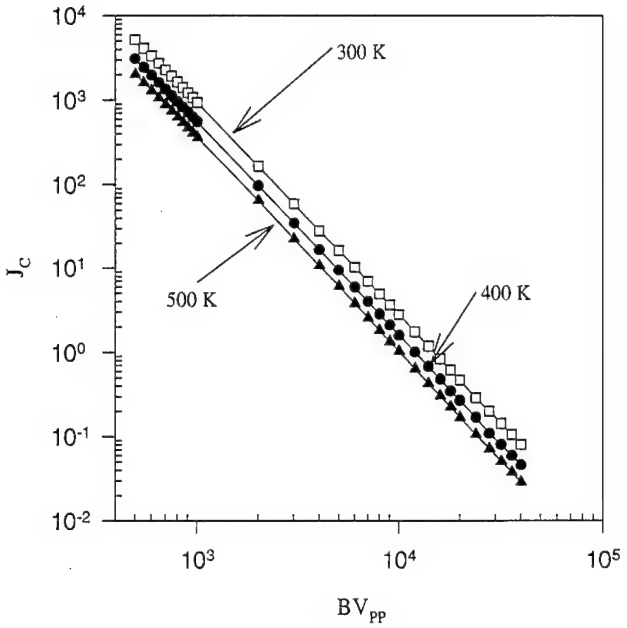

Fig. 6 : Variation of cross-over current density for 6H-SiC unipolar and 6H-SiC bipolar devices with voltage-rating and temperature of operation.

Temperature (K)	4H-SiC unipolar Vs Si bipolar
300	$J_C = 1.258 \times 10^{11} (BV_{PP})^{-2.5}$
400	$J_C = 7.76 \times 10^{10} (BV_{PP})^{-2.5}$
500	$J_C = 4.4 \times 10^{10} (BV_{PP})^{-2.5}$

(a)

Temperature (K)	6H-SiC unipolar Vs Si bipolar
300	$J_C = 1 \times 10^{10} (BV_{PP})^{-2.5}$
400	$J_C = 5.76 \times 10^{9} (BV_{PP})^{-2.5}$
500	$J_C = 3.4 \times 10^{9} (BV_{PP})^{-2.5}$

(b)

Temperature (K)	4H-SiC unipolar Vs 4H-SiC bipolar
300	$J_C = 3.7 \times 10^{11} (BV_{PP})^{-2.5}$
400	$J_C = 2.1 \times 10^{11} (BV_{PP})^{-2.5}$
500	$J_C = 1.35 \times 10^{11} (BV_{PP})^{-2.5}$

(c)

Temperature (K)	6H-SiC unipolar Vs 6H-SiC bipolar
300	$J_C = 2.9 \times 10^{10} (BV_{PP})^{-2.5}$
400	$J_C = 1.7 \times 10^{10} (BV_{PP})^{-2.5}$
500	$J_C = 1.1 \times 10^{10} (BV_{PP})^{-2.5}$

(d)

Table 2 (a-d) : Numerically derived relations for variation of cross-over current density with voltage-rating and temperature of operation for unipolar and bipolar devices.

C.2. Analysis of forward voltage drop at 100 A / cm^2

The forward voltage drop (V_F) for a unipolar device and bipolar device, for a given voltage rating (BV_{PP}), at a given current density can be calculated using equations (1) and (2) respectively. Figure 7 shows the typical variation of V_F with BV_{PP} for unipolar and bipolar devices. In unipolar devices, the forward voltage drop depends on the drift-region resistance. The drift-region resistance increases as the breakdown voltage increases, since the doping decreases resulting in a gradual increase in the forward voltage drop with the voltage-rating of the device. In bipolar devices there is conductivity modulation of the drift-region and the forward voltage drop is nearly the same for all voltage-ratings. The voltage rating at which the two curves intersect will be defined as the cross-over breakdown voltage BV_C. For voltage ratings lesser than BV_C unipolar devices have a lower V_F than bipolar devices and for voltage ratings greater than BV_C bipolar devices have a lower V_F than unipolar devices . The forward voltage drop for 4H-SiC unipolar devices and silicon bipolar devices at a current density of 100 A / cm^2 at 3 different temperatures (300 K, 400 K, 500 K), as a function of the voltage rating (BV_{PP}) are shown in figure 8. As the temperature, increases the forward voltage drop in unipolar devices increases due to degradation of mobility while the forward voltage drop in bipolar devices decreases slightly with increase in temperature. Hence the V_F versus BV_{PP} curves for 4H-SiC unipolar devices shift up as the temperature increases whereas the curves for silicon bipolar devices remain nearly unchanged. It can be seen that at 300 K, the value of BV_C is approximately 4500 V. This implies that 4H-SiC unipolar devices have a lower V_F than silicon bipolar devices for voltage ratings upto 4500 V. Figure 9 shows a similar plot for 6H-SiC unipolar devices and silicon bipolar devices. The cross-over breakdown voltage in this case is approximately 1000 V as against 4500 V in the previous case. This is due to the fact that the electron mobility along the c-axis in 6H-SiC is nearly 10 times lower than that in 4H-SiC. Similar plots for 4H-SiC unipolar and 4H-SiC bipolar devices are shown in figure 10 and the value of BV_C at 300 K is approximately 7000 V. Figure 11 shows a similar plot for 6H-SiC unipolar and 6H-SiC bipolar devices. The values of BV_C at different temperatures are given in table 3.

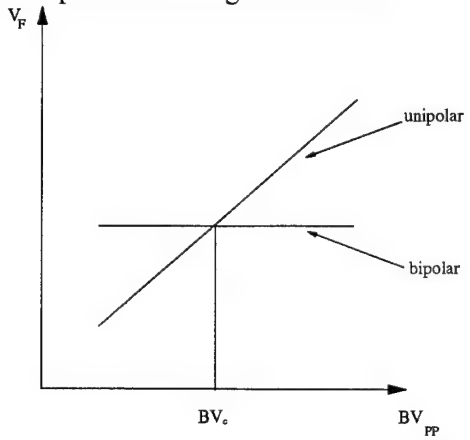

Fig. 7 : Typical variation of forward voltage drop (V_F) with the voltage-rating (BV_{PP}) for unipolar and bipolar devices, the voltage-rating at which the two curves intersect is called the cross over breakdown voltage (BV_C).

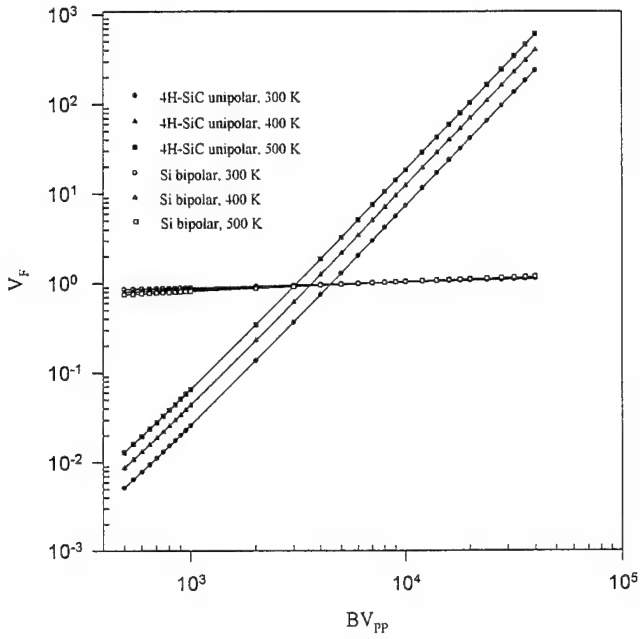

Fig. 8 : Variation of V_F (at 100 A / cm^2) with voltage-rating for 4H-SiC unipolar and silicon bipolar devices at 3 different temperatures.

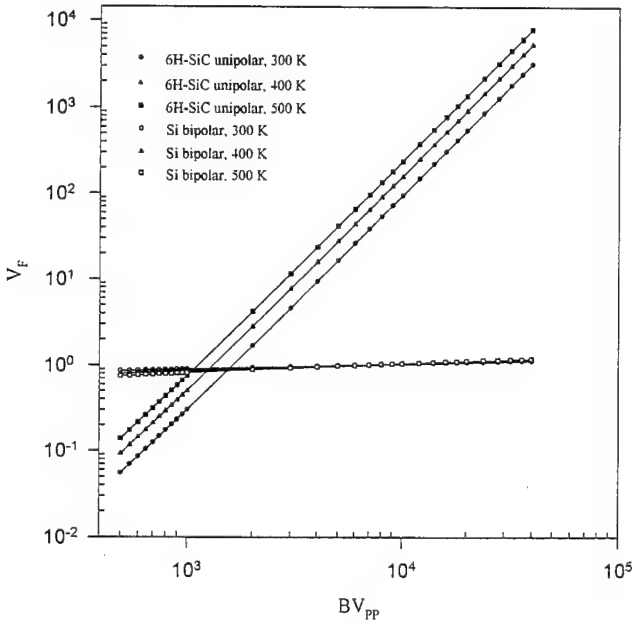

Fig. 9 : Variation of V_F (at 100 A / cm^2) with voltage-rating for 6H-SiC unipolar and silicon bipolar devices at 3 different temperatures.

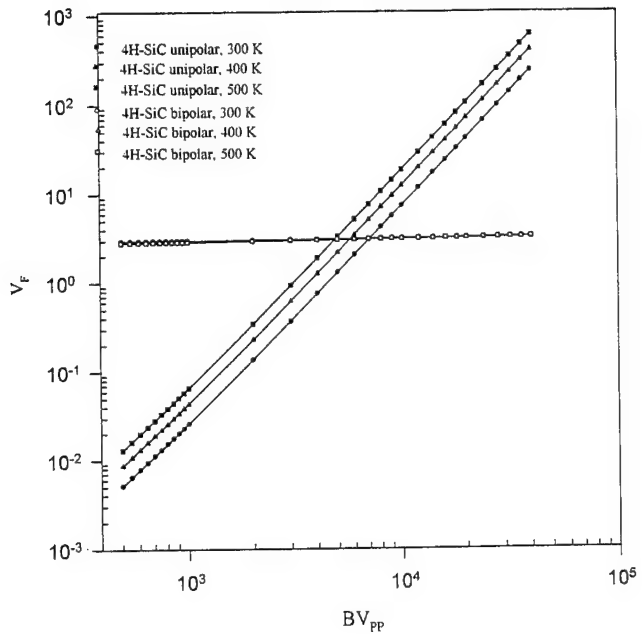

Fig. 10 : Variation of V_F (at 100 A / cm^2) with voltage-rating for 4H-SiC unipolar and 4H-SiC bipolar devices at 3 different temperatures.

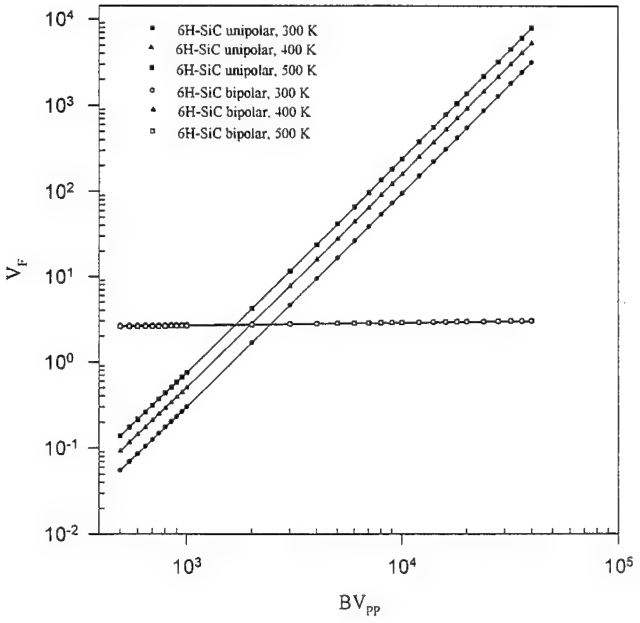

Fig. 11 : Variation of V_F (at 100 A / cm^2) with voltage-rating for 6H-SiC unipolar and 6H-SiC bipolar devices at 3 different temperatures.

Material / Temperature	4H-SiC / Si	6H-SiC / Si	4H-SiC/4H-SiC	6H-SiC/6H-SiC
300 K	4500 V	1800 V	7000 V	2500 V
400 K	3500 V	1200 V	5500 V	2000 V
500 K	3000 V	1050 V	4500 V	1800 V

Table 3 : Cross-over breakdown voltages for unipolar Vs bipolar devices for 4H-SiC, 6H-SiC, Si at different temperatures of operation.

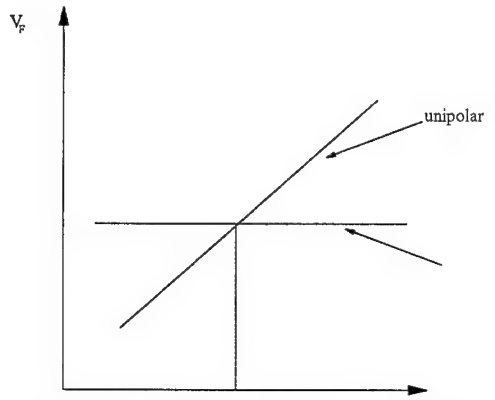

Fig. 12 : Variation of V_F with temperature for unipolar and bipolar devices, the temperature at the point of intersection of these curves is defined to be the cross-over temperature (T_C)

For a given breakdown voltage, the forward voltage drop for unipolar devices increases with temperature while that for bipolar devices decreases. Figure 12 shows a typical variation of the forward voltage drop with temperature for unipolar and bipolar devices. The temperature at which the V_F versus T curves for unipolar and bipolar devices intersect will be defined as the cross-over temperature (T_C). The values of T_C as a function of the breakdown voltage (BV_{PP}) for 4H-SiC unipolar and silicon bipolar devices are plotted in figure 13. Similar plots for 6H-SiC unipolar and silicon bipolar devices, 4H-SiC unipolar and bipolar devices, 6H-SiC unipolar and bipolar devices are also shown in the same figure. At a given voltage-rating, if the temperature of operation of the device is going to be less than T_C then a unipolar device will have a lower forward voltage drop than a bipolar device. If the temperature of operation is more than T_C then the bipolar device will have a lower forward voltage drop. The value of T_C at 3000 V for 4H-SiC unipolar devices to silicon bipolar devices is approximately 500 K. Thus for a voltage-rating of 3000 V if the temperature of operation of the device is going to be less than 500 K then 4H-SiC unipolar devices will be preferred over silicon bipolar devices as they will have a lower forward voltage drop.

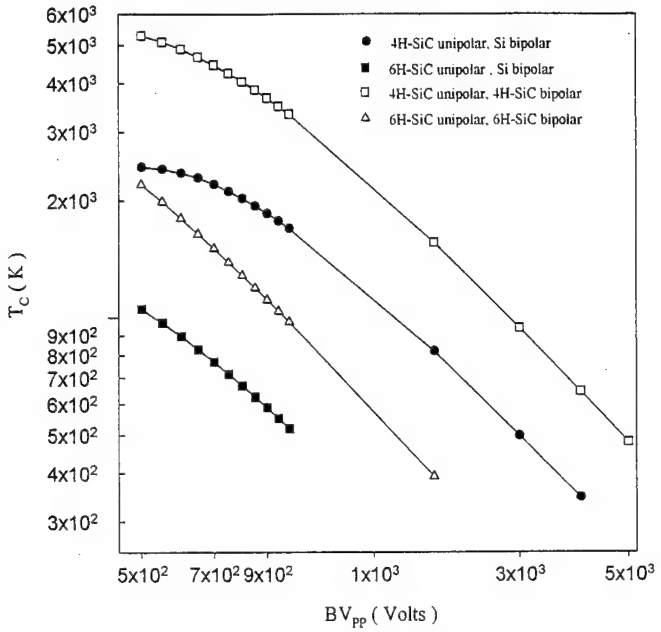

Fig. 13 : Variation of cross-over temperature with the voltage-rating of the device, if the temperature of operation is below the cross-over temperature unipolar devices have a lower V_F than bipolar devices.

D. Conclusions

A first order analysis to compare the performance of unipolar devices to bipolar devices over a range of voltage-ratings (500 V - 40000 V) was performed. The forward voltage drop at 100 A / cm^2 was used to do the comparison. It was found that for room temperature operation, 4H-SiC unipolar devices have lower forward voltage drops than silicon bipolar devices for voltage ratings upto 4500 V.

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[6] William J. Schaffer, G.H. Negley, K. G. Irvine, and J. W. Palmour, " Conductivity Anisotropy in Epitaxial 6H and 4H SiC," *Mat. Res. Soc. Symp. Proc.* Vol. 339 pp. 595-600, 1994.

III. Analysis of the U-MESFET

A. Introduction

From the discussion in the previous section, it is evident that silicon carbide unipolar power devices are preferable for voltage ratings below 4500 V. The most commonly used unipolar device in silicon power device technology is the power MOSFET. In this section the current status of silicon carbide MOSFETs and associated problems are presented. The alternatives to the power MOSFET are the JFET and the MESFET. The output characteristics of a 1000 V silicon carbide MESFET are analyzed using simulations.

B. Background

B.1 Power MOSFET

The two commonly used MOSFET structures are the DMOSFET and the UMOSFET shown in figures 1 (a) and 1 (b) respectively. In both the MOSFET structures, the p-n junction between the P-base region and the N-drift region provides the blocking capability. Due to the very small diffusion rate of dopants in silicon carbide, it is not practical to fabricate the DMOSFET [1]. The most suitable structure is the U-MOSFET in which the P-base region is epitaxial grown on the N-drift layer. The power MOSFET is capable of blocking voltage in only one quadrant. For n-channel structures the devices are operated with a positive voltage applied to the drain. When the gate electrode is shorted to the source the device can support a large drain voltage across the P-base/N-drift region junction. The forward blocking capability is shown in figure 2 by the lowest trace [2].

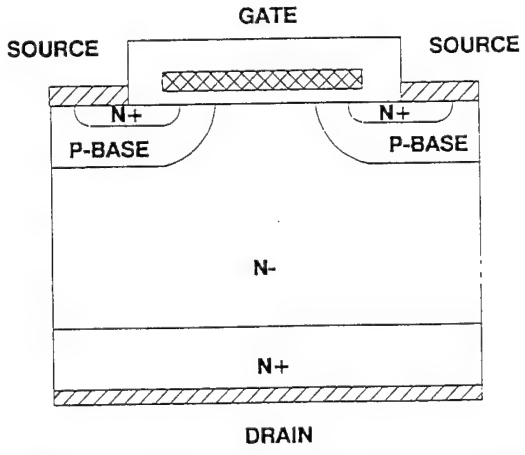

Fig.1 (a) : Cross Section Of a D-MOSFET

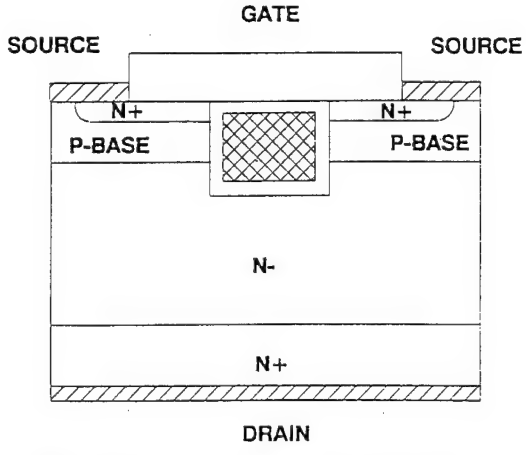

Fig. 1 (b) : Cross Section Of a U-MOSFET

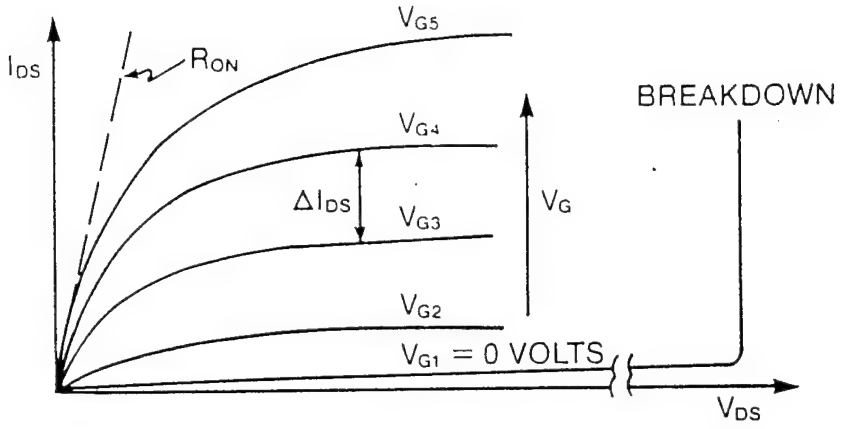

Fig. 2 : Output characteristics of a typical MOSFET, the forward blocking capability is shown by the lowest trace.

When a positive gate bias is applied, the channel becomes conductive. At low drain voltages the current flow is resistive with the on-resistance determined by a combination of the channel and drift region resistances. The total on-resistance decreases with increasing gate-bias until it approaches a constant value. At high drain voltages, the resistance of the power MOSFET increases and ultimately the current saturates at high drain voltages as shown in figure 2.

B.2.Problems with SiC MOSFETs

The UMOSFET on-resistance consists mainly of the channel resistance and the drift-region resistance[2]. The channel resistance ($R_{ch,sp}$) is given by :

$$R_{ch,sp} = \frac{L_{ch} (W_m + W_t)}{2 \mu_{ns} C_{ox} (V_G - V_T)} \qquad (1)$$

where L_{ch} is the length of the channel, W_m and W_t are the trench and mesa-widths respectively, C_{ox} is the capacitance per unit area of the gate oxide, V_G and V_T are the gate and threshold voltages and μ_{ns} is the inversion channel mobility [2]. In order to achieve an on-resistance value close to the ideal value, the channel resistance should be made as low as possible. Hence it is important to obtain a high inversion channel mobility.

The inversion channel mobilities reported in silicon carbide are very low (20 cm^2/V-s) [3], resulting in severe degradation of specific on-resistances. This is illustrated in figure 3 where the calculated specific on-resistance is given as a function of the breakdown voltage for various inversion layer mobility values [1]. Further the critical electric field for breakdown in silicon carbide is approximately 5 x 10^6 V/cm and since the field in the oxide will be about thrice the field in the underlying silicon carbide, the electric field in the oxide can reach its breakdown strength of 1 x 10^7 V/cm at the trench corners, as shown in figure 4, leading to rupture of the gate oxide and premature breakdown of the

device[1]. Due to these problems, MOSFETs cannot be used to realize the potential of silicon carbide as a superior replacement to silicon. Hence, it is important to investigate other unipolar structures like the JFET and the MESFET shown in figures 5 (a) and 5(b) respectively. However the fabrication of a SiC JFET is impractical due to the high energies required to implant the p^+ gate. The MESFET needs a good Schottky contact to be formed between the metal and semiconductor in order to achieve good forward blocking. Schottky rectifiers with high blocking capabilities (400 V-1000 V) and reasonably low leakage currents have been reported on both 4H-SiC and 6H-SiC [4-6]. Hence the vertical MESFET (U-MESFET) structure was chosen for investigation.

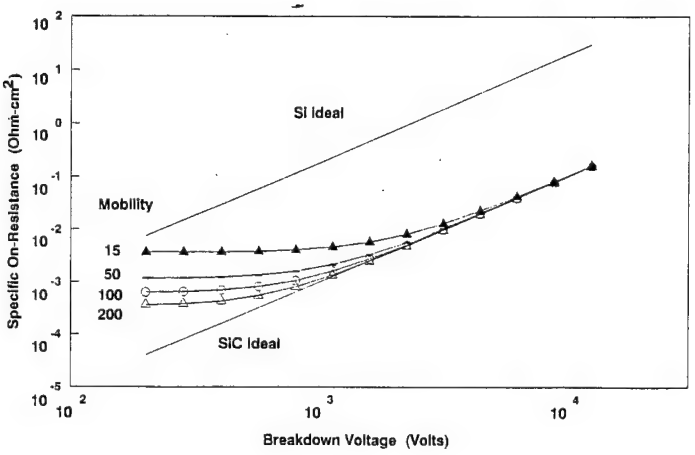

Fig. 3 : Variation of Specific On-resistance with breakdown voltage and inversion layer mobilities for a SiC MOSFET.

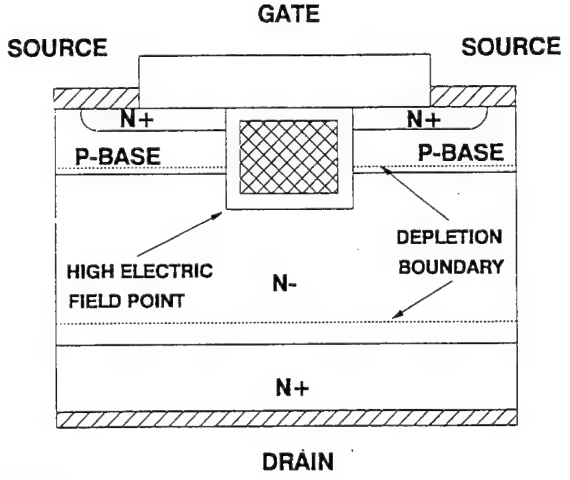

Fig.4 : Electric Field Crowding at the trench corner in a SiC U-MOSFET can cause premature breakdown of the oxide layer.

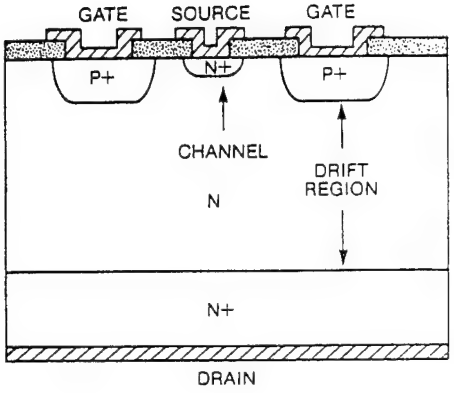

Fig. 5 (a) : Cross Section Of a JFET, the gate is formed by P^+diffusion or implant into the N-epilayer.

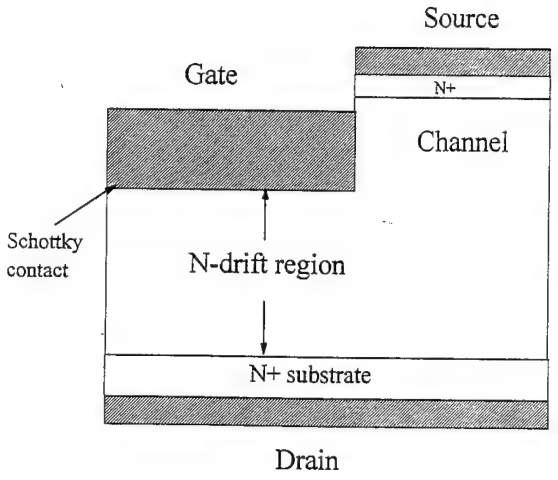

Fig. 5 (b) : Cross-section of a U-MESFET, the Schottky gate is formed in a trench.

C. U-MESFET

C.1 Basic Operation

Fundamentally, the MESFET consists of a bar of semiconductor material whose resistance can be controlled by the application of a reverse-bias voltage to a gate region. A U-MESFET (metal-semiconductor field effect transistor) is shown in figure 5 (b). The gate is a Schottky junction, formed in a trench in order to isolate it from the source. In the absence of a gate bias, that is, with the gate short-circuited to the source, the current flow between drain and source is limited by the resistance of the lightly doped N-type region

between these current carrying terminals. The N-type region consists of two portions, the region between the junction gates is called the channel and the region below the junction gates is called the drift region. The resistances of both these regions add together to determine the total resistance to current flow between the drain and source terminals.

With the application of a reverse gate bias with respect to the source (negative voltage to the gate terminal), a depletion region forms around the gate junctions and extends out into the channel. Since the depletion region is devoid of free carriers, the resistance of the channel region increases with the application of higher reverse gate bias voltages. By use of the gate junction depletion layer, the resistance of the MESFET can be altered by changing the reverse gate bias voltage. Thus, the MESFET is a voltage-controlled device. In the MESFET, the gate bias supply needs to provide only a small displacement current to modulate the depletion region width, resulting in a high input impedance.

C.2 Forward Blocking

The resistance of the MESFET is controlled by changing the channel conductivity. In a MESFET designed for operation at high drain voltages, it is necessary to include a wide drift-region. During the application of large drain voltages in the forward blocking mode, the voltage is supported across the gate depletion layer. This depletion layer extends down from the gate junction toward the drain. The drift region doping concentration and thickness should be designed to support the drain-gate voltage, that is, the sum of the absolute values of the drain and gate voltages, because they combine to determine the total reverse bias across the gate Schottky junction. It should also be noted that the gate-source structure must be capable of supporting the highest gate-source voltage.

In the forward blocking mode, the depletion layers from the gate junctions extend through the entire channel. The applied reverse gate bias sets up a potential barrier in the channel. For current to flow between drain and source, electrons must surmount this potential barrier. As the drain voltage increases the potential barrier is lowered and electron injection becomes easier [7].

C.2.1 Triode like characteristics of the U-MESFET

The channel length in a U-MESFET is determined by the depth of the trench. In silicon carbide, due to the slow etch rates, the practical trench-depths are ≤ 3 μm. Thus for a silicon carbide U-MESFET, the channel length would be typically the same as the channel width. For these devices, the potential barrier established in the channel by the reverse gate bias extends over only a small vertical distance. As the drain voltage is increased, the drain potential penetrates into the channel and lowers the potential barrier. At low drain voltages, the potential barrier established by the gate voltage is pronounced and extends throughout the channel. When the drain voltage is increased, the potential barrier is pulled down by the drain potential in regions of the channel away from the gate region. Electron injection can now occur in these regions. Since the injection of carriers across the potential barrier varies exponentially with the barrier height, the drain current exhibits a rapid increase once the potential barrier is reduced. The resulting triode like

characteristics, that is, drain current continuously increasing with increasing drain voltage, of MESFETs with short channel length are illustrated in figure 6. [7].

C.2.2 Blocking Gain

An important parameter for devices with triode like characteristics is the voltage blocking gain. The DC blocking gain can be defined as

$$G_B = \frac{V_{DS}}{V_{GS}} \qquad (2)$$

where V_{DS} is the maximum voltage blocked by a gate-bias V_{GS}. It is crucial to achieve a large blocking gain in high-voltage MESFETs for two reasons : (1) a higher blocking gain reduces the gate drive voltage that must be supplied by the gating circuit to achieve any desired forward blocking capability, and (2) a higher blocking gain reduces the total voltage that must be supported by the gate junction. The total reverse bias across the gate junction is given by

$$V_{RJ} = (V_{DS} + V_{GS}) = V_{DS}\left(1+\frac{1}{G_B}\right) \qquad (3)$$

A large blocking gain reduces the breakdown voltage that must be designed for the gate junctions.

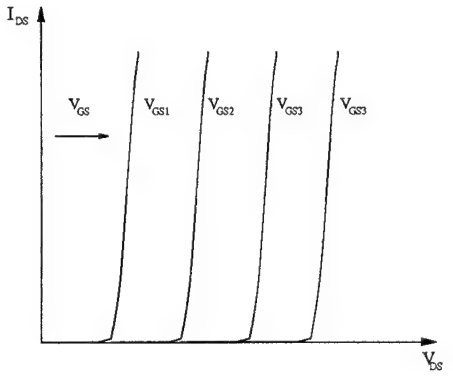

Fig. 6 : Triode like Output Characteristics Of the MESFET.

C.2.3 Forward Conduction, On-Resistance

The U-MESFET is a normally-on device and conducts current through the channel when a positive bias is applied to the drain with all the other terminals at zero bias. The on-resistance of the U-MESFET is the resistance between the source and drain terminals in the on-state. The on-resistance is an important device parameter because it determines the maximum current rating. The power dissipation in the U-MESFET, during the on-state is given by:

$$P_D = I_D V_D = I_D^2 R_{on} \qquad (4)$$

Expressed in terms of the chip area (A):

$$\frac{P_D}{A} = J_D^2 R_{on,sp} \qquad (5)$$

where (P_D / A) is the power dissipation per unit area; J_D is the on-state current density; and $R_{on,sp}$ is the *specific on-resistance*, defined as the on-resistance per unit area. For a given power dissipation the operating current density varies inversely as the square root of the specific on-resistance [2].

The specific on-resistance of the power U-MESFET is determined by the resistance components illustrated in figure 7 for the U-MESFET structure. Thus:

$$R_{on} = R_{CS} + R_{N^+} + R_R + R_J + R_D + R_S + R_{CD} \qquad (6)$$

where R_{N+} is the contribution from the N^+ source implant, R_R is the resistive component just under the source implant, R_J is the contribution from the drift region between the Schottky gates, R_D is the drift region resistance and R_S is the substrate resistance. Additional resistances can arise from non-ideal contact (R_{CS} and R_{CD}) between the source/drain metal and the N^+ semiconductor regions as well as the leads used to connect the device to the package. Each of these contributions is described below.

Substrate resistance: The contribution from the substrate is generally negligible for high-voltage MESFETs. It can be assumed that the current density is uniform within the substrate because of rapid current spreading at the drift region interface. The specific on-resistance contributed by the substrate is then given by:

$$R_{S,sp} = \rho_s t_s \qquad (7)$$

where ρ_s is the resistivity of the substrate and t_s is its thickness. Typically $R_{S,sp}$ is of the order of $1x10^{-4}$ Ω-cm^2.

Source Resistance: The resistance per cm^2 due to the N^+ source is given by:

$$R_{N+,sp} = \frac{\rho_{N+} L_{N+} (W_t + W_m)}{W_m} \qquad (8)$$

where ρ_{N+} is the sheet resistance of the N^+ source, L_{N+} is the thickness of the N^+ contact region, W_t is the trench-width and W_m is the mesa-width as shown in figure 7. Typically $R_{N+,sp}$ is of the order of 1×10^{-7} Ω-cm^2.

R_R is the resistance of the region under the N^+ source and just above the channel and is given by:

$$R_{R,sp} = \frac{\rho_D (t_d - L - L_{N+} - W_D)(W_t + W_m)}{W_m} \qquad (9)$$

where ρ_D is the drift region resistivity, L is the gate length and W_D is the depletion width due to contact potential of the Schottky gate. Typically $R_{R,sp}$ is in the order of $1x10^{-5}$ Ω-cm^2.

Channel Resistance :The channel resistance in U-MESFETs is similar to the JFET region resistance in the D-MOSFET [2]. The channel resistance per cm^2 for the structure shown in figure 7 is given by :

$$R_{J,sp} = \frac{\rho_D (W_t + W_m)(L + 2W_D)}{(W_m - 2W_D)} \qquad (10)$$

For $W_t = W_m = 1$ μm with the channel doping of the order of $1x10^{16}$ cm^{-3}, the channel resistance is of the order of $1x10^{-4}$ Ω-cm^2.

Drift Region Resistance: In this analysis, the drift region is assumed to begin below the bottom of the trench as indicated in figure 7. The current spreads from the channel region into the drift region. Many possible models for the current spreading into the drift region can be proposed. One such model that allows a reasonably accurate estimation of the drift region spreading resistance, is based on the current spreading from a cross-section of ($a = W_m - 2W_D$) at a 45 degree angle[8]. The current flow paths overlap at a depth $W_G / 2$ below the trench bottom and the drift region resistance can be modeled as the sum of a region where the cross-section for current flow increases with depth and a second region with uniform cross-section equal to the cell-width. This leads to a drift region specific resistance given by:

$$R_{D,sp} = \frac{\rho_D (W_t + W_m)}{2} \ln\left[\frac{W_m - 2W_D + W_t}{W_m - 2W_D}\right] + \rho_D (t - t_d - \frac{W_t}{2}) \qquad (11)$$

Typically $R_{D,sp}$ is in the order of 10^{-4} Ω-cm^2, for a voltage-rating of 1000 V.

Thus the channel resistance and drift-region resistance are the main components that determine the specific on-resistance of the U-MESFET.

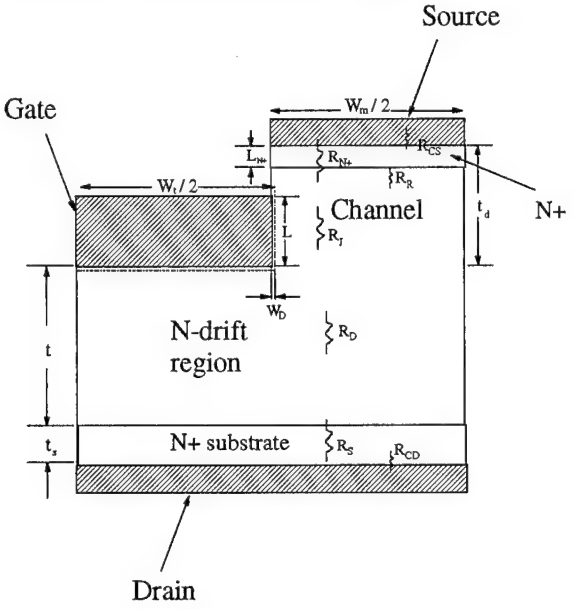

Fig. 7 : Cross Section Of the U-MESFET illustrating the various components of On-Resistance.

D. SiC U-MESFET : Numerical Simulations

Two-dimensional numerical simulations of the U-MESFET shown in figure 7 were performed using *TMA-MEDICI* to analyze the performance of the device. The electron drift mobility in 4H-SiC, along the c-axis, is nearly 10 times higher than that in 6H-SiC [9]. Hence 4H-SiC was used in the simulations as the specific on-resistance will be lower for 4H-SiC devices.

D.1 Design Variations studied using simulations

The blocking gain of the U-MESFET depends on the gate-bias needed to pinch-off the channel. A thin channel can be pinched off with a low gate-bias resulting in a high blocking gain whereas a wide channel will result in a lower blocking gain. In order to study the variation of blocking gain with the channel width, the mesa-widths (W_m) of the simulated structures was varied from 1 μm - 3 μm, the ratio W_t/W_m was fixed at 1 for all the cases. The N^- region doping was varied from $1x10^{16}$ cm^{-3} - $2x10^{16}$ cm^{-3}, the gate-length (L) was varied from 0.5 μm-1 μm and the trench-depth (t_d) was fixed at 1.5 μm. The N^+ implant for source contact was fixed at 0.2 μm . Since titanium is known to form good Schottky contact to 4H-SiC [4], the simulations were performed with titanium as the metal for the Schottky gate. This was done by specifying the work function of the metal contact to be 4.77 eV. A design variation with gold (work function = 5.3 eV) as the Schottky gate was also simulated, in order to study the variation of blocking gain and on-state resistance with the type of metal used to form the Schottky gate.

D.2 Variation of potential barrier in the channel

Figure 8 shows the potential barrier in the channel region for a gate bias (V_{GS}) of -20 V and a drain bias (V_{ds}) of 50 V, for the different simulated structures, with L = 1 μm and a doping of $1x10^{16}$ cm^{-3}. It can be seen that for a given gate-length, the barrier is maximum for the structure with the smallest mesa-width and decreases with increasing mesa-width. This is due to the fact that the gate-bias needed to pinch off a smaller mesa-width is smaller. A similar plot with L = 1 μm and W_m, W_t = 1 μm for two different dopings of $1x10^{16}$ cm^{-3} and $2x10^{16}$ cm^{-3} is shown in figure 9. It can be seen that the structure with lower doping has a higher potential barrier. This is due to the fact that a low doped channel can be pinched off with a smaller gate-bias. The variation of the potential barrier with the gate-length is illustrated in figure 10. It can be seen that the barrier reduces as the gate-length decreases. The variation of potential barrier in the channel for different Schottky contacts (Ti, Au) is shown in figure 11. It can be seen that the Schottky gate with gold as the metal has a higher barrier, this is due to the fact that gold forms a Schottky contact with a higher barrier height than titanium [4-5] and hence higher contact potential which results in the channel getting pinched off at a lower gate bias than that is needed for a titanium gate. Thus the gate-bias needed to turn-off the device depends on the mesa-width, gate-length, channel doping and the work function of the gate metal.

D.3 Forward Blocking Characteristics

The simulated triode-like blocking characteristics for the structures with doping of $1x10^{16}$ cm^{-3}, gate-length of 1μm, with a titanium gate, with the mesa-widths varying from 1μm to 3μm are shown in figures 12(a)-12 (d). Since the doping and epi-layer thickness is fixed for all the cases, the forward blocking voltage and the gate bias needed to achieve the blocking are determined by the potential barrier in the channel region. As is expected, the structure with the smallest mesa-width (1 μm) needs the least gate voltage (-10 V) to achieve the rated blocking voltage of 1200 V, whereas the structure with W_m = 3 μm is able to block only 350 V even with a gate-bias of -100 V.

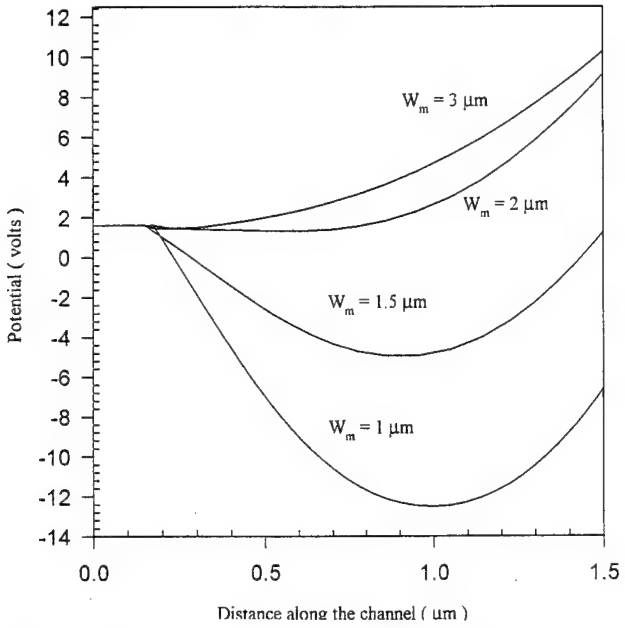

Fig. 8 : For a given doping ($1x10^{16}$ cm^{-3}) and gate-length (1 µm), the potential barrier in the channel increases as the mesa-width decreases. V_{GS} = -20 V, V_{DS} = 50 V

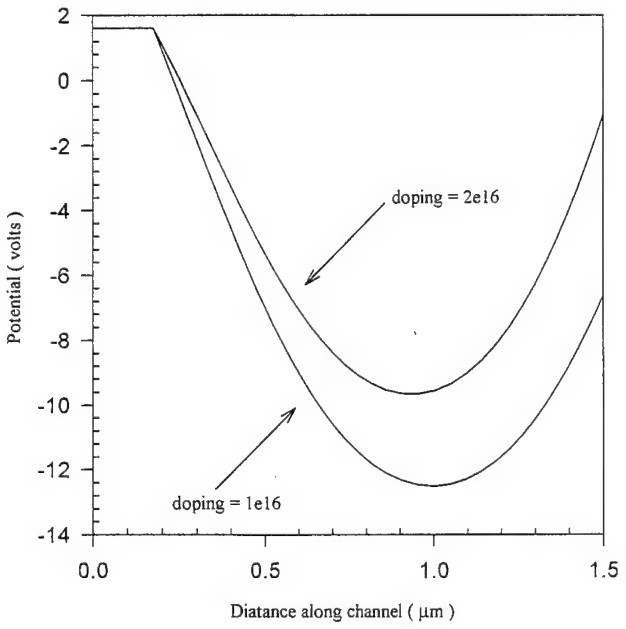

Fig. 9: For a fixed gate-length (1µm) and mesa-width (1µm) the potential barrier in the channel increases as the doping is reduced. V_{GS} = -20 V, V_{DS} = 50 V.

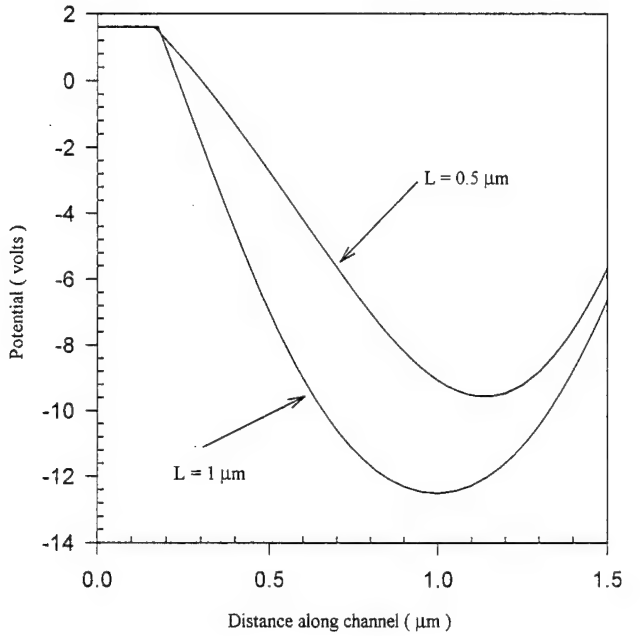

Fig. 10 : For a fixed mesa-width (1μm) and doping ($1x10^{16}$ cm^{-3}) the potential barrier in the channel decreases as the gate-length decreases. V_{GS} = -20 V, V_{DS} = 50 V.

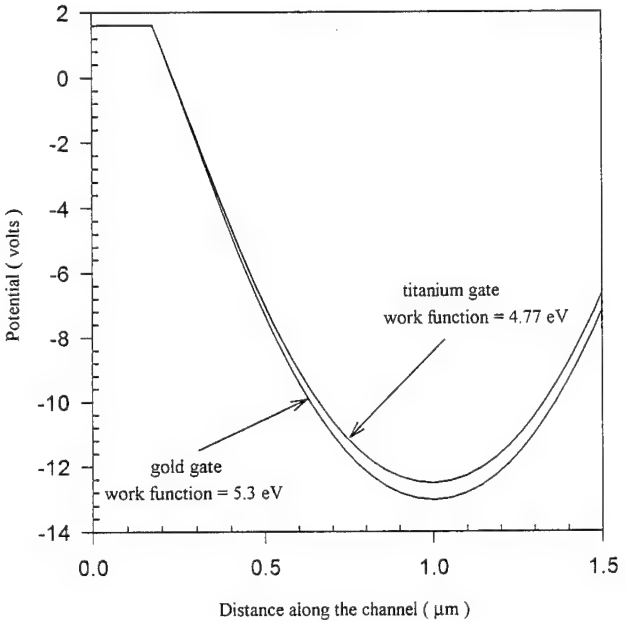

Fig. 11 : For a given mesa-width (1μm), gate-length (1μm) and doping ($1x10^{16}$ cm^{-3}) the potential barrier in the channel increases with the work function of the gate metal. V_{GS} = -20 V, V_{DS} = 50 V

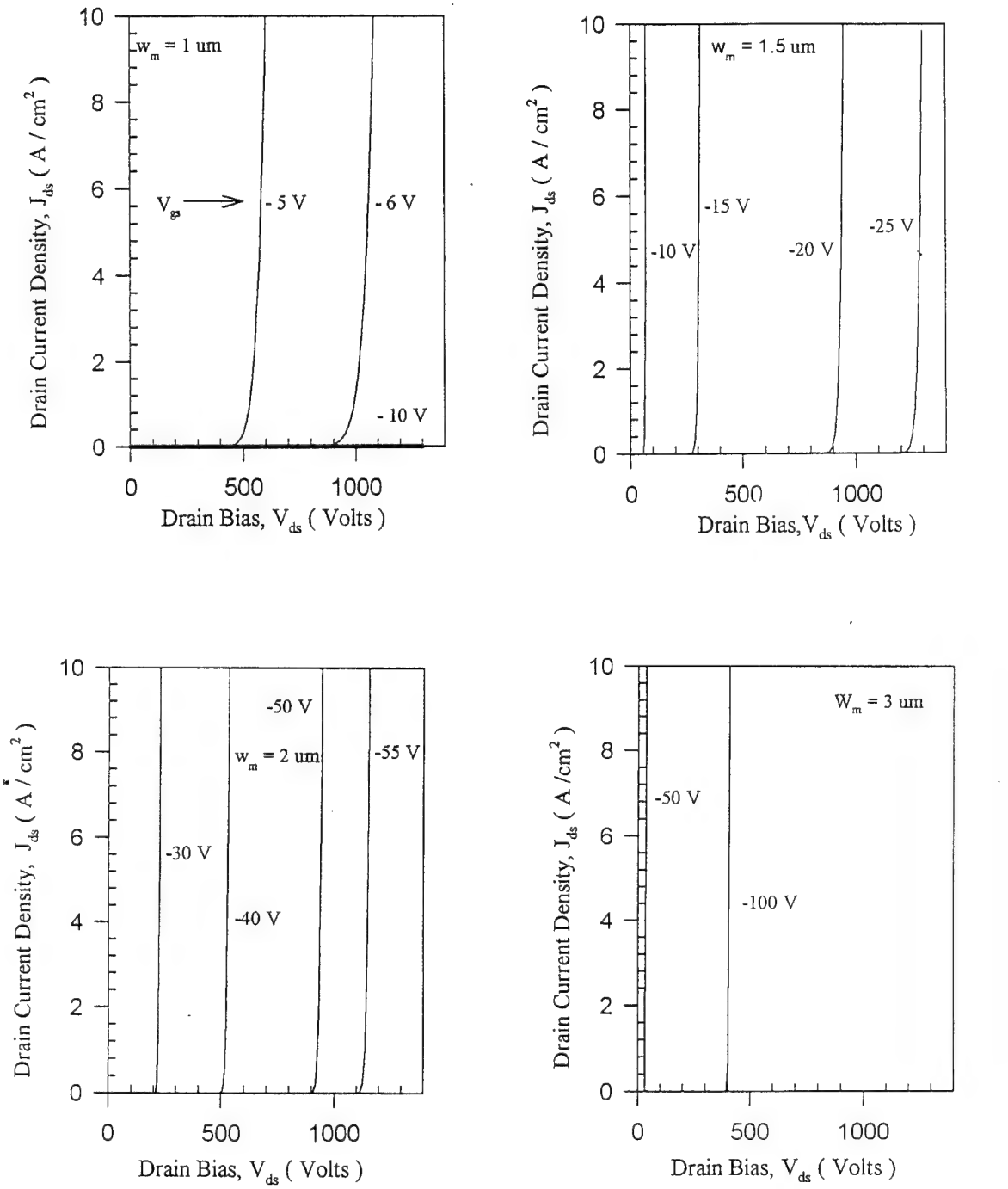

Fig.12 (a-d) : Forward blocking characteristics of the U-MESFET with different mesa-widths. The structure with the smallest mesa-width needs the lowest gate-bias to achieve the rated blocking voltage.

D.4 Electric Field Distribution

The three-dimensional electric field distributions for the structure with W_m = 1μm and W_m = 1.5 μm at a drain bias of 1200 V are shown in figure 13(a) and 13(b). It can be seen that there is electric-field crowding at the trench corners. This crowding causes premature breakdown in U-MOSFETs as the field in the oxide will be thrice that in the semiconductor [1], but the U-MESFET does not have any such problems and is able to block the rated voltage.

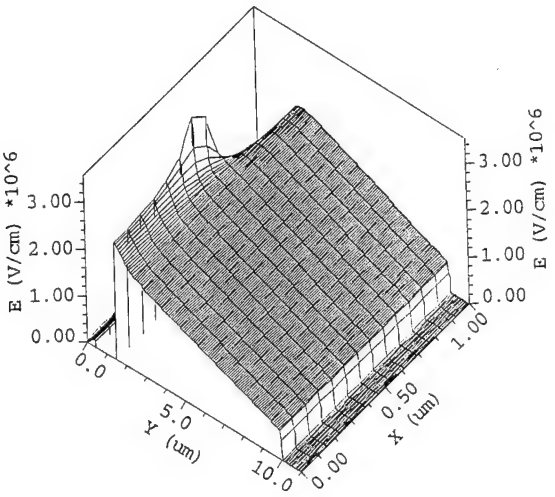

Fig. 13 (a) : Three-Dimensional Electric Field Distribution at V_{gs} =-10 V and V_{ds} = 1200 V for structure with W_m = 1 μm and doping = $1x10^{16}$ cm^{-3}

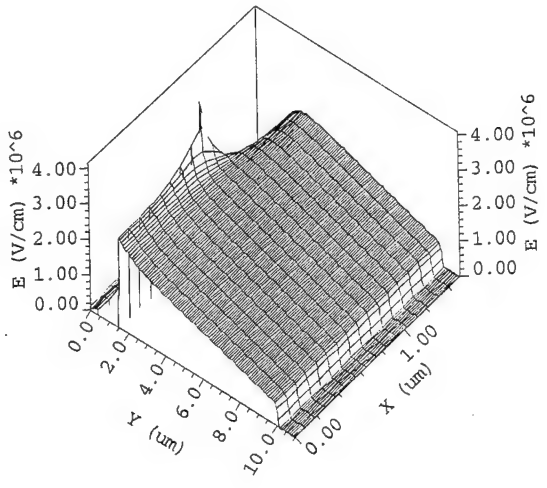

Fig. 13 (b) : Three-Dimensional Electric Field Distribution at V_{gs} =-25 V and V_{ds} = 1200 V for structure with W_m = 1.5 μm and doping = $1x10^{16}$ cm^{-3}.

D.5 Specific On-Resistance, Blocking Gain

As discussed earlier the U-MESFET is a normally-on device. The on-state characteristics of the U-MESFET was simulated at a gate-bias of 0 V and the specific on-resistance at 100 A / cm^2 for the different structures was computed. The specific on-resistance, the maximum blocking voltage, the gate-bias required to achieve blocking and the DC-blocking gains for the different structures that were simulated are summarized in table (1). It can be seen that the blocking gain is higher for structures with smaller mesa-widths and longer gate-lengths. The blocking gain varied from a maximum of 120 for the structure with W_m = 1 μm to a low value of 3.5 for the structure with W_m = 3 μm. The ideal value of the specific on-resistance for the simulated structures is also shown in table 1. The ideal value for specific on-resistance is taken to be just the drift-region resistance ($\rho_D t$). The specific on-resistance is lower (and closer to the ideal value) for the structures with larger mesa-widths. This is due to the fact that a smaller fraction of the mesa-width is depleted by the contact potential (V_{bi}) of the Schottky gate junction. This is illustrated in figure 14 where the current flowlines at an on-state current density of 100 A / cm^2 are shown for structures with different mesa-widths. The current however spreads out rapidly resulting in a low specific on-resistance (close to the ideal value) in all the structures. The specific on-resistance values extracted from simulation are compared with the values calculated using the analytical expressions (derived earlier), in table 2, it can be seen that the simulation results agree well with the analytical model.

Structure #	W_m (μm)	W_t (μm)	L (μm)	$V_{ds,\,max}$ (volts)	V_{gs} (volts)	G_B	$R_{on\text{-}sp}$ (Ω-cm^2) simulated	$R_{on\text{-}sp}$ (Ω-cm^2) ideal
1	1	1	1	1200	10	120	9.6×10^{-4}	5.4×10^{-4}
2	1.5	1.5	1	1200	25	48	8.6×10^{-4}	5.4×10^{-4}
3	2	2	1	1140	55	20.7	8.35×10^{-4}	5.4×10^{-4}
4	3	3	1	350	100	3.5	7.95×10^{-4}	5.4×10^{-4}
5*	1	1	1	800	10	80	4.45×10^{-4}	2.92×10^{-4}
6	1	1	0.5	1200	15	80	8.75×10^{-4}	5.7×10^{-4}
7+	1.5	1.5	1	1200	24	50	9.3×10^{-4}	5.4×10^{-4}

*structure 5 has an epi-layer doping of 2×10^{16} cm^{-3}, all other structures have dopings of 1×10^{16} cm^{-3}
+structure 7 has gold as the Schottky contact for the gate, all other structures are with titanium as the Schottky contact

Table 1 : Table summarizing the specific on-resistances and blocking gains of the various structures simulated.

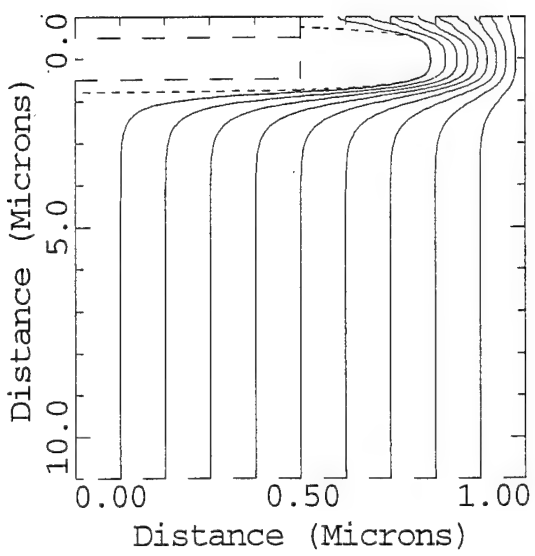

Fig. 14 (a) : W_m = 1 μm

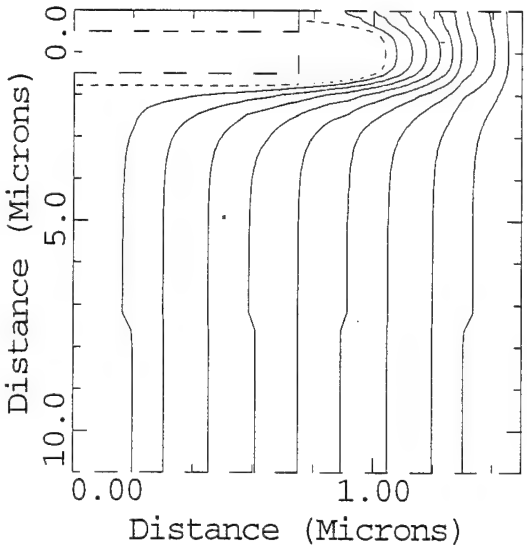

Fig. 14 (b) : W_m = 1.5 μm

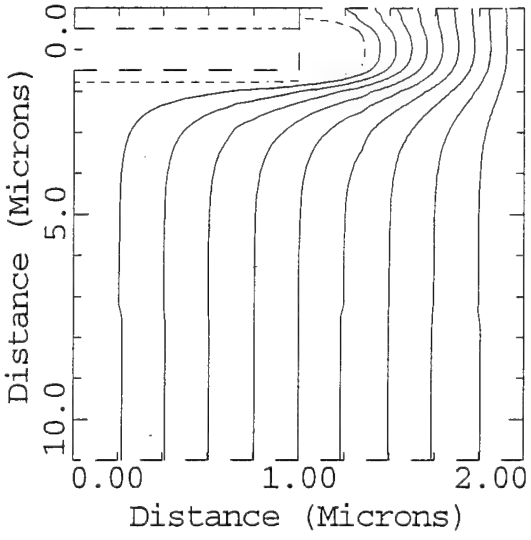

Fig. 14 (c) : W_m = 2 μm

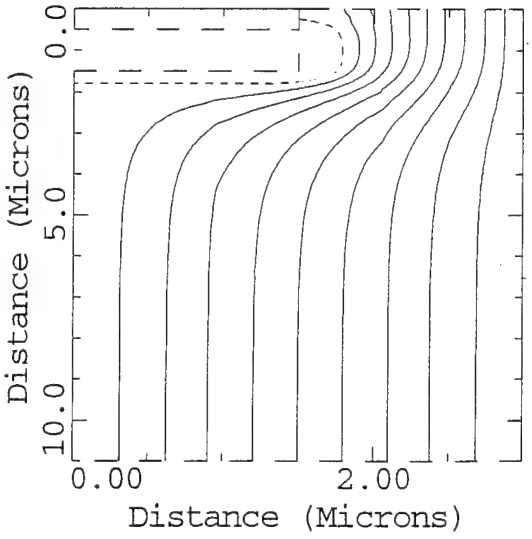

Fig. 14 (d) : W_m = 3 μm

Fig. 14 (a-d) : The fraction of the channel depleted at zero gate-bias decreases with increasing mesa-width, resulting in lower specific on-resistance. The current flowlines spread uniformly in the drift region resulting in a low on-resistance, close to the ideal value, for all the structures. The doping for all the structures shown is 1 x 10^{16} cm^{-3} and the gate metal is titanium.

*Structure #	R_{on-sp} (Ω-cm^2) simulated	R_{on-sp} (Ω-cm^2) calculated
1	9.6×10^{-3}	1.1×10^{-3}
2	8.6×10^{-4}	9.4×10^{-4}
3	8.35×10^{-4}	8.8×10^{-4}
4	7.95×10^{-4}	8.6×10^{-4}
5	4.45×10^{-4}	4.8×10^{-4}
6	8.75×10^{-4}	9.5×10^{-4}
7	9.3×10^{-4}	9.8×10^{-4}

*Structure numbers correspond to the same designs as in table 1

Table 2 : The specific on-resistance values extracted from simulation agree well with the values calculated using analytical models.

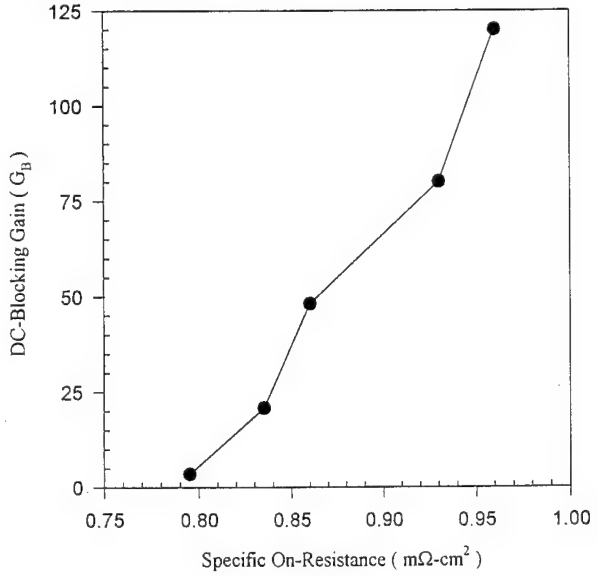

Fig. 15 : The trade-off between obtaining a high blocking gain at the cost of increased on-resistance.

In order to obtain a high blocking gain, it is necessary to pinch off the channel with a low gate bias. This can be done by using a small mesa-width, larger gate-length, lower doping or a Schottky gate with a higher contact potential. All of these result in a

higher specific on-resistance. The trade-off between obtaining a higher blocking gain at the cost of increased on-resistance is illustrated in figure 15.

E. Conclusions

It is evident from the above discussion that the U-MESFET is a suitable device to realize the potential of SiC as a superior replacement to silicon. It was seen that the structure with the lowest mesa-width (1 μm) has the best blocking gain (G_B = 120) and needs only 10 V gate bias to achieve the rated blocking voltage of 1200 V. However the on-resistance for this structure is the highest (9.6 x $10^{-4}\Omega$-cm^2). Also from a fabrication point of view, it is difficult to get mesa-widths of 1μm. The structure with 1.5 μm mesa-width needs 25 V gate bias to achieve the rated blocking voltage, a blocking gain of 48, and has a lower on-resistance (8.6 x 10^{-4} Ω-cm^2). While the on-resistance decreased for higher mesa-widths the blocking gain reduced rapidly and the structure with 3 μm mesa-width had a DC-blocking gain of only 3.5. **Thus the structure with mesa-width of 1.5 μm is the optimum design in terms of high blocking gain, low on-resistance and ease of fabrication.** Fabrication of the U-MESFET however involves filling at least 1.5 μm deep trenches with metal which is difficult, it is also difficult to obtain isolation between the gate and source metal which involves extremely critical alignments.

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[1] B. Jayant Baliga, "Trends in Power Semiconductor Devices," *IEEE Transactions on Electron Devices*, vol.43, No.10, pp.1717-1731, 1996.

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[4] R. Raghunathan, D. Alok and B. J. Baliga, " High Voltage 4H-SiC Schottky Barrier Diodes," *IEEE Electron Device Letters*, vol.16, No.6, pp.226-227, 1995.

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IV. Fabrication of the HJFET

A. Introduction

As discussed in section III, the U-MESFET is an excellent device to realize the potential of silicon carbide as a replacement to silicon bipolar devices. However, the fabrication of a U-MESFET involves filling deep trenches with metal which is difficult. Further, for a metal gate, it is tough to obtain a good isolation between the gate and the source. In this section, a novel trench gate heterojunction field effect transistor (HJFET) (whose operation is identical to that of the U-MESFET) is analyzed. The process for fabricating the HJFET is presented. The HJFET shown in figure 1 has a P^+-polysilicon gate instead of the metal gate in the U-MESFET. Gate to source isolation is obtained by oxidizing the polysilicon before the source metallization. The fabrication of the HJFET involves a six mask level process with no critical alignments.

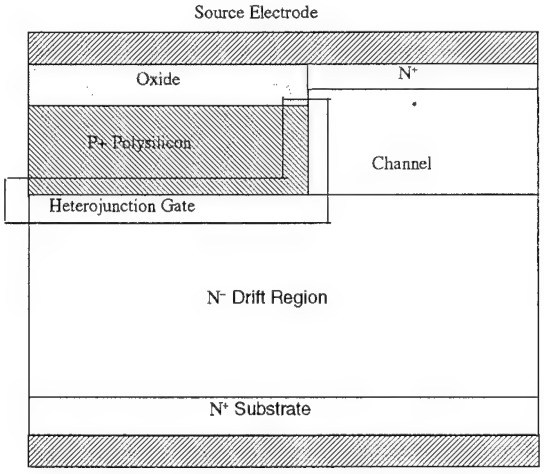


Fig. 1 : Cross-section of the HJFET, the polysilicon gate is oxidized to obtain isolation between the gate and source.

B. Process/Fabrication Sequence

The starting material for the fabrication of the HJFET was a [0001] oriented N^+ -SiC substrate (~300 μm thick) with an N-epitaxial layer (1×10^{16} cm^{-3}), with thickness of 10 μm. Two wafers , one of poly-type 4H and the other of poly-type 6H were used. The baseline process sequence is schematically illustrated in figure 2.

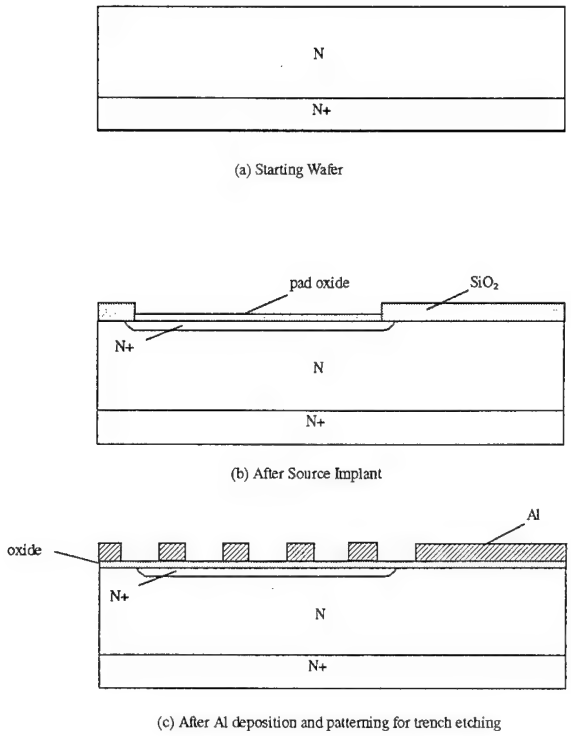


Fig. 2 : Process sequence of the HJFET

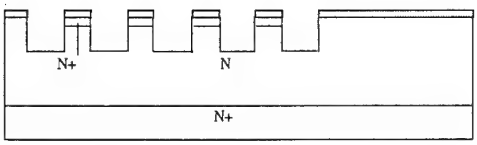
B.1 N^+ implant for the source contact

The first masking level was used for nitrogen implantation followed by high temperature annealing to obtain a shallow (~0.2 μm) N^+ region at the surface for the source contact. A 0.8 μm thick oxide layer was deposited by CVD and patterned by using a buffered oxide etch. A 0.2 μm thick pad oxide was then deposited by CVD. The nitrogen implantation and anneal were performed. The conditions were as follows :

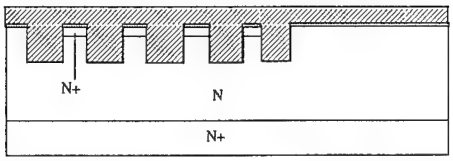
- Two successive implants with a dose of $1x10^{15}$ cm^{-2} and energies of 30 keV and 40 keV respectively.
- High temperature anneal was performed in a nitrogen ambient at 1250 °C for 30 min. to activate the dopants.

B.2 Removal of thick oxide

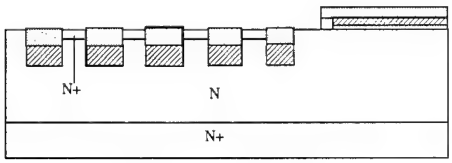
The second masking level was used to remove the entire oxide in areas outside the area with alignment marks and for certain devices designed with oxide under the source pad. A 0.2 μm thick oxide was deposited by CVD, to act as etch-stop during the poly etch back (described later).



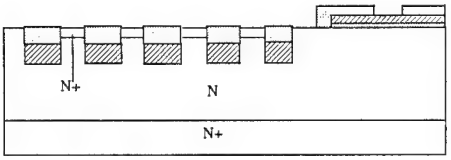
(d) After RIE and wet etch of Al mask



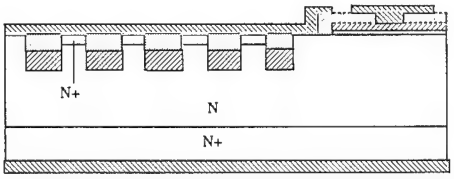
(e) After Poly Deposition



(f) After Poly etch-back & Oxidation



(f) After Contact etching



(g) After Final Al metallization and patterning

Fig. 2 : Process sequence of the HJFET (cont)

B.3 Trench etching and polysilicon refill

The third masking level was used to define the trench regions. Aluminum was used as the mask to etch trenches. The Al was patterned using lift-off lithography. 1.5 μm deep trenches were etched in SiC using RIE. The process used for RIE etches both SiC and oxide at the same rate and the 0.2 μm oxide was etched in the same step. The RIE was performed at the Microelectronics laboratory at NCSU and the conditions and the chemistry were as follows :

- Gases used, flow rates : SF_6 (9 sccm), O_2 (1 sccm).
- Chamber pressure : 50 mtorr
- Cathode temperature : 20 °C
- Power : 120 W
- The 1" SiC wafer was placed on the backside of a 4" Si wafer and a Teflon sheet with a 3" hole in the center was used to cover the aluminum cathode completely.
- The etch rate for SiC was ~ 150 A / s

It was found that the bottom surface of the trenches was rough, as shown in figure 3. This could cause the P^+-polysilicon / N-SiC heterojunction to have bad reverse I-V characteristics.

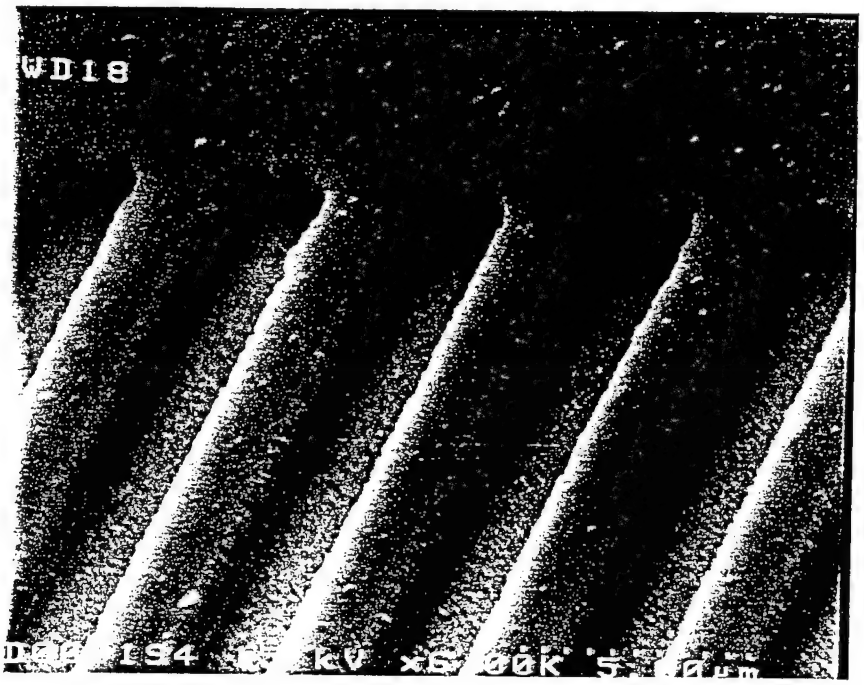


Fig.3: SEM micrograph of the wafer surface after trench-etching showing the roughness at the bottom of the trenches.

The Aluminum was then removed by wet chemical etching and 4 μm of undoped polysilicon was deposited to refill the trenches conformally. The polysilicon was then uniformly doped P-type by boron implantation and an anneal in nitrogen ambient to drive in the implant to get a uniform doping of approximately $1x10^{19}$ cm^{-3}. The polysilicon was deposited at Philips Research Laboratories, NY and the boron implant and anneal were done at MCNC. The conditions for the polysilicon deposition, the boron implantation and drive in were as follows:

- Polysilicon Deposition : 625 °C, SiH_4
- Boron implantation : Energy = 100 keV, dose = 2×10^{16} cm^{-2}
- Drive-in : 1250 °C for 4hr. in a nitrogen ambient.

B.4 Polysilicon etch back :

The fourth masking level was used to protect the polysilicon in the gate pad regions, before the polysilicon etch back for planarization. The polysilicon etch back was done using RIE at the microelectronics laboratory at NCSU. The etch rate for polysilicon was ~1750 A / s and the RIE was done for 27 min. to remove the entire polysilicon on the mesa regions. The conditions and chemistry for the RIE are as follows :

- Gases used, flowrates : SF_6 (15 sccm), O_2 (5 sccm)
- Chamber pressure : 60 mtorr
- Cathode temperature : 20 °C
- Power : 100 W

The polysilicon etch was non-uniform across the surface of the wafer, this would result in variation of the gate-lengths across the wafer surface.

In order to ensure that the mesa region of the silicon carbide does not get etched during this step, a 0.2 μm thick oxide was deposited by CVD prior to etching trenches. After the polysilicon etch back, the polysilicon in the trench was oxidized to obtain gate to source isolation. At this step, it is necessary to ensure that enough of the polysilicon inside the trench is oxidized such that there is no polysilicon in contact with the N^+-SiC in the mesa region, as this would result in gate to source shorts. Wet oxidation for 2.5 hours at 1000 °C was performed to oxidize the polysilicon. The oxidation rate for SiC is much lower than that for polysilicon and only 100 A (approximately) of oxide was grown on the mesa region whereas there was about 8000 A of oxide grown in the trench region. The wafers were now subjected to an unmasked BOE (buffered oxide etch) dip for 40 s to etch the oxide on the mesa region, while retaining sufficient amount of oxide in the trench region to provide gate to source isolation.

B.5 Contact to the polysilicon gate

The fifth masking level was used to define the contact holes to the P^+- polysilicon gate pads. Photoresist was used as the mask and the wafers were subjected to a 13 minute BOE dip to etch away the oxide grown on the polysilicon (in the previous step) to open contact holes for the gate metal. At the end of the fourth step, polysilicon etch back and

oxidation, 4 μm thick polysilicon patterns for the gate pads were left. The photoresist spun on to the wafers could not cover the 4 μm step properly. Hence some of the oxide along the sidewalls of the polysilicon pads was etched during the contact hole etch. This could result in gate to source shorts, since the source metal runs over the sidewalls of the polysilicon pads as shown in figure 4.

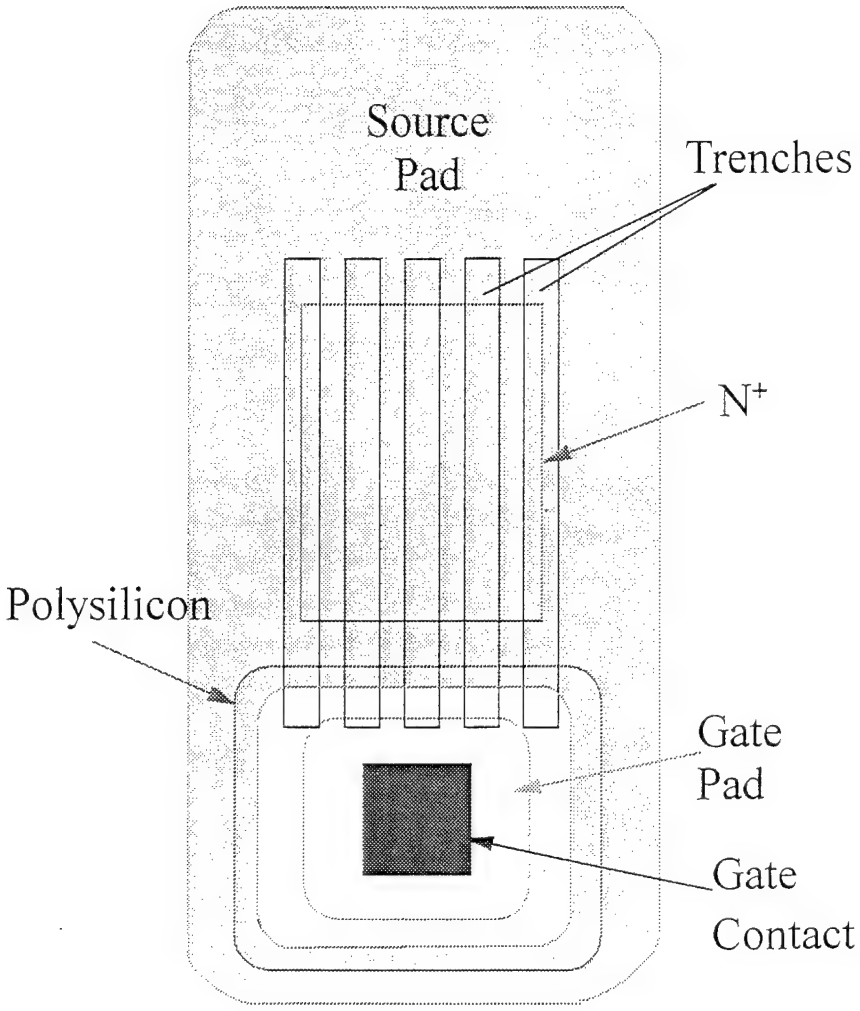


Fig. 4 : Mask Design for the HJFET. The source metal runs over the oxide on the polysilicon pad, if the oxide at the sidewall of the pad is etched during contact hole etching it would result in gate to source shorts.

B.6 Metallization

The sixth masking level was used to define the source and gate metal pads. The patterning was done by lift-off lithography. Negative photoresist was patterned on the wafer prior to the metallization. Both the front and backside metallizations involved sequential evaporation of 2000 A of Ti followed by 8000 A of Al.

B.7 Edge Termination

The edge termination for the P^+- polysilicon / N-SiC heterojunction was designed to be a Schottky contact followed by an argon ion implant to terminate the Schottky contact. The argon ion implantation has been shown to be an ideal termination technique for Schottky contacts [1]. As shown in the mask design in figure 4, the source metal (Ti) runs over the oxide on the polysilicon (grown in step 4) and forms a Schottky contact to the N-SiC surface.

C. Conclusions

The process for fabricating the HJFET is fairly simple and does not involve any critical alignments. The trench etching in SiC resulted in trenches with roughness at the bottom. This could cause the heterojunction gate to have a high leakage current. The polysilicon etch back was non-uniform and would result in variation of the gate-length from die to die across the wafer. The step coverage of the polysilicon pads by photoresist in the fifth masking level was poor and this could result in gate to source shorts. The polysilicon should be subjected to an unmasked etch prior to a masked etch so that the polysilicon pad is only about 1-1.5 μm thick in which case step coverage could be more easily achieved.

References:

[1] D. Alok, B. J. Baliga and P. K. McLarty, "A simple edge termination for silicon carbide devices with nearly ideal breakdown voltage," *IEEE Electron Device Lett.*, vol. 15, pp. 394-395, 1994.

V. Experimental Results, Conclusions and Future work

A. Introduction

In this section, the results of the experimental measurements on the HJFET fabricated on 4H-SiC are discussed. The conclusions from the fabrication and characterization of the HJFET are presented and suggestions for the future work are outlined.

B. Experimental Results

As discussed in section IV, in the fifth mask level of the HJFET process, the isolation oxide was etched away, due to bad photoresist step coverage of the polysilicon gate pads. This resulted in gate to source shorts. Hence, the triode-like blocking characteristics of the HJFET could not be experimentally observed. However, the HJFET showed current-saturation in the on-state due to channel pinch-off. Also the channel resistivity could be modulated at small gate-bias steps. The specific on-resistance of the HJFET was very low and close to the expected value.

B.1 On-Resistance

For the purposes of this analysis, the ideal specific on-resistance of the drift-region could be obtained using a $N^+/N^-/N^+$ test element fabricated in the HJFET process. The J-V curves of this test element and the different fabricated HJFET structures (at $V_{GS} = 0$ V) are shown in figure 1. The values of $R_{on,sp}$, calculated using the measured resistances are summarized in table 1. As expected the on-resistance of the HJFET decreases as the mesa-width (W_m) increases and the trench-width (W_t) decreases. The $N^+/N^-/N^+$ structure had an $R_{on,sp}$ of 1.74 mΩ-cm^2. The structure with W_m = 2 μm and trench-width (W_t)= 1 μm had the lowest $R_{on,sp}$ of 2.43 mΩ-cm^2 and is very close to the ideal value. The structure with W_m = 1 μm and W_t = 3 μm had an $R_{on,sp}$ of 9.68 mΩ-cm^2 which is about 9 times higher than the expected value. These values are 100 times better than values reported for SiC MOSFETs [1] demonstrating that the HJFET is a very promising structure for power switch development.

B.2 Forward-blocking :

The HJFET is a normally-on device and needs a negative potential between the gate and source in order to pinch-off the channel to provide forward blocking capability. However, due to the gate to source shorts, the device could not be turned-off. Inspite of this problem, it was found that the HJFET structures with narrow channel widths (W_m = 1 - 1.5 μm) exhibited current saturation in the on-state due to the channel being pinched-off by the drain bias. In addition despite the gate to source shorts, the channel resistivity could be modulated at small gate-biases (between -0.2 V to 0.2 V). The pentode-like [2] characteristics of the HJFET at low drain voltages are shown in

figures 2-4. From these characteristics it can be observed that the structure with $W_m = 1$ μm saturates at a drain current of 0.01 A, which is much lower than the saturation current of 0.08 A for the structure with $W_m = 1.5$ μm.

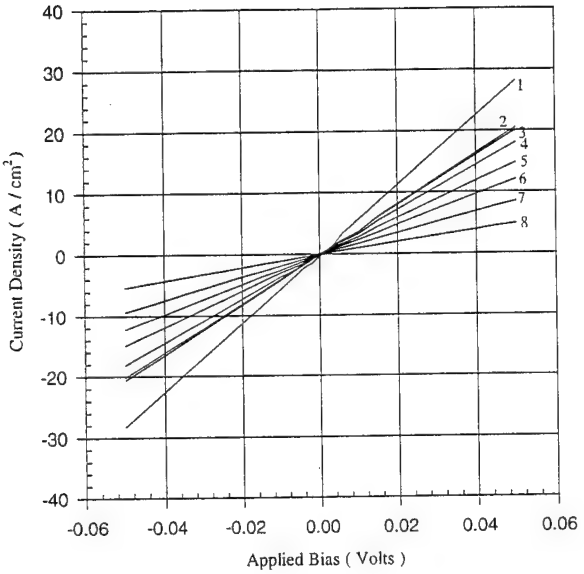


Fig. 1 : J-V characteristics to determine the $R_{on,sp}$ of the different HJFET structures

Curve (#)	mesa-width (W_m, μm)	trench-width (W_t, μm)	$R_{on,sp}$ (mΩ-cm^2)
1*	-	-	1.74
2	2	1	2.43
3	3	3	2.48
4	2.5	3	2.7
5	2	3	3.38
6	1.5	3	4.1
7	1	1	5.54
8	1	3	9.68

*This curve is for the $N^+ / N^- / N^+$ test element.

Table 1 : $R_{on,sp}$ of the different HJFET structure fabricated, the curve# corresponds to the curve in fig.1

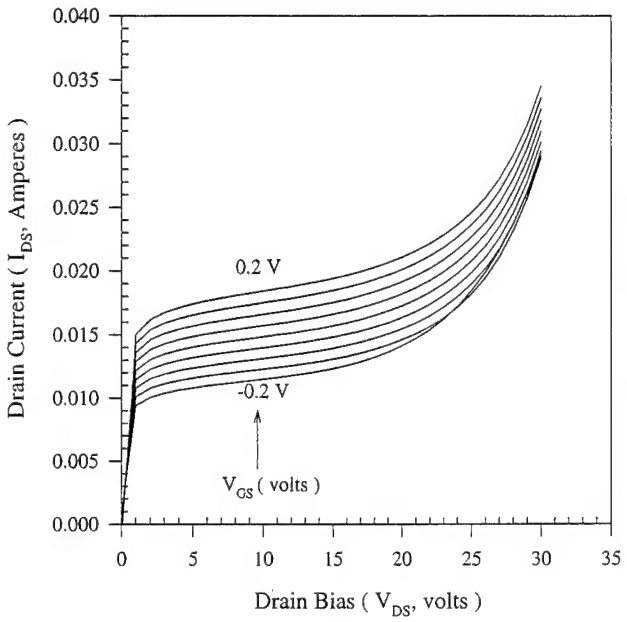


Fig. 2 : Pentode-like characteristics of the fabricated HJFET, W_m = W_t = 1 μm, the gate-bias is increased in steps of 50 mV.

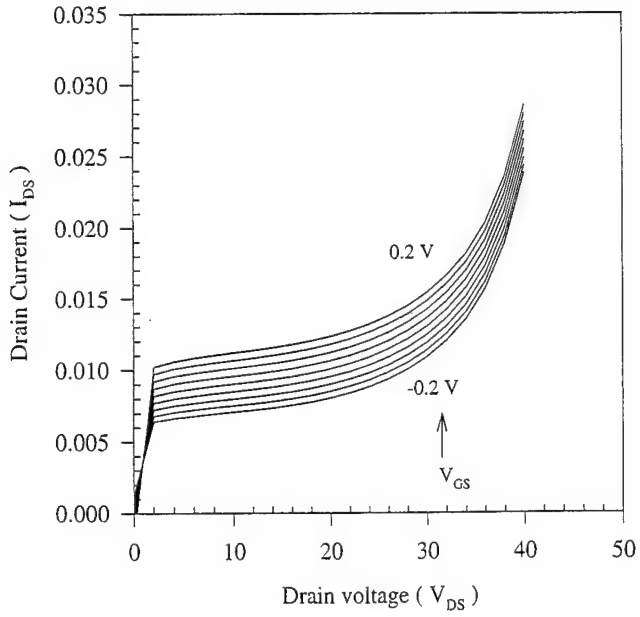


Fig. 3 : Pentode-like characteristics of the fabricated HJFET, W_m = 1, W_t = 3 μm, the gate-bias is increased in steps of 50 mV.

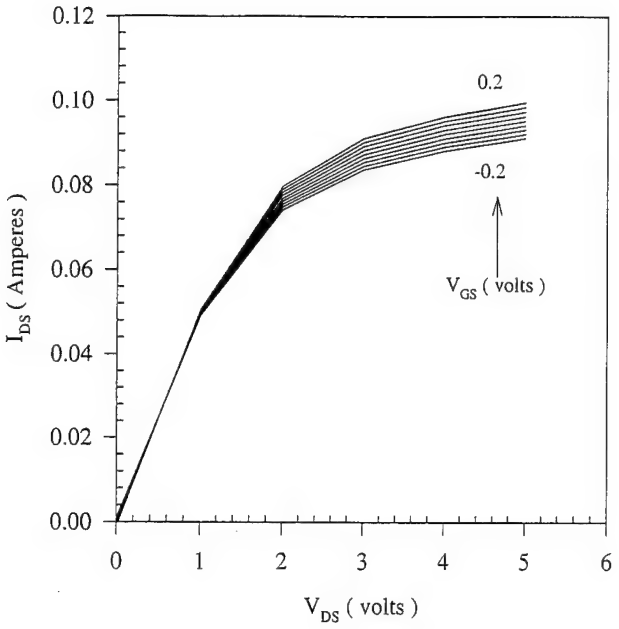


Fig. 4 : Pentode-like characteristics of the fabricated HJFET, W_m = 1.5, W_t = 3 μm, the gate-bias is increased in steps of 50 mV.

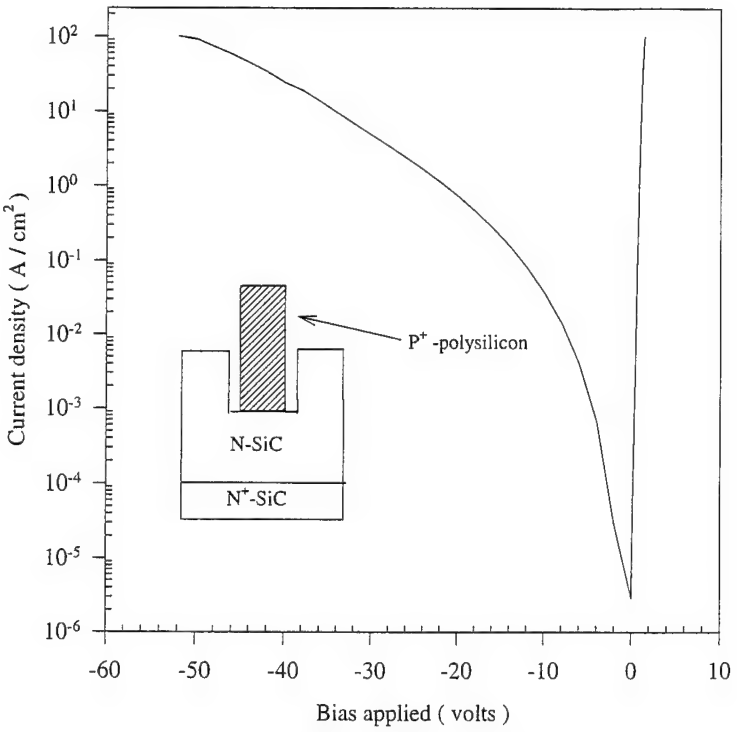


Fig. 5 : J-V characteristics of the heterojunction diode, the leakage currents are high due to the bad interface caused by the roughness at the trench bottom.

B.3 Measurements on test elements

A heterojunction diode structure was also fabricated with the HJFET structures to study the properties of the P^+-polysilicon / N-SiC heterojunction. The J-V characteristics of the heterojunction diode are shown in figure 5 demonstrating that the diode shows reasonably good rectification. However the leakage current density of the diode is quite high. This could be due to the roughness at the bottom of the trenches in SiC as described in section IV.

A Ti Schottky rectifier was also fabricated with the HJFET to verify the blocking capability of the material. This diode showed excellent J-V characteristics and blocked about 240 V in the reverse direction, which is the expected breakdown voltage for unterminated Schottky diodes[3]. The forward voltage drop for the diode was 0.8 V at 100 A / cm^2 The J-V characteristics of the Schottky rectifier are shown in figure 6.

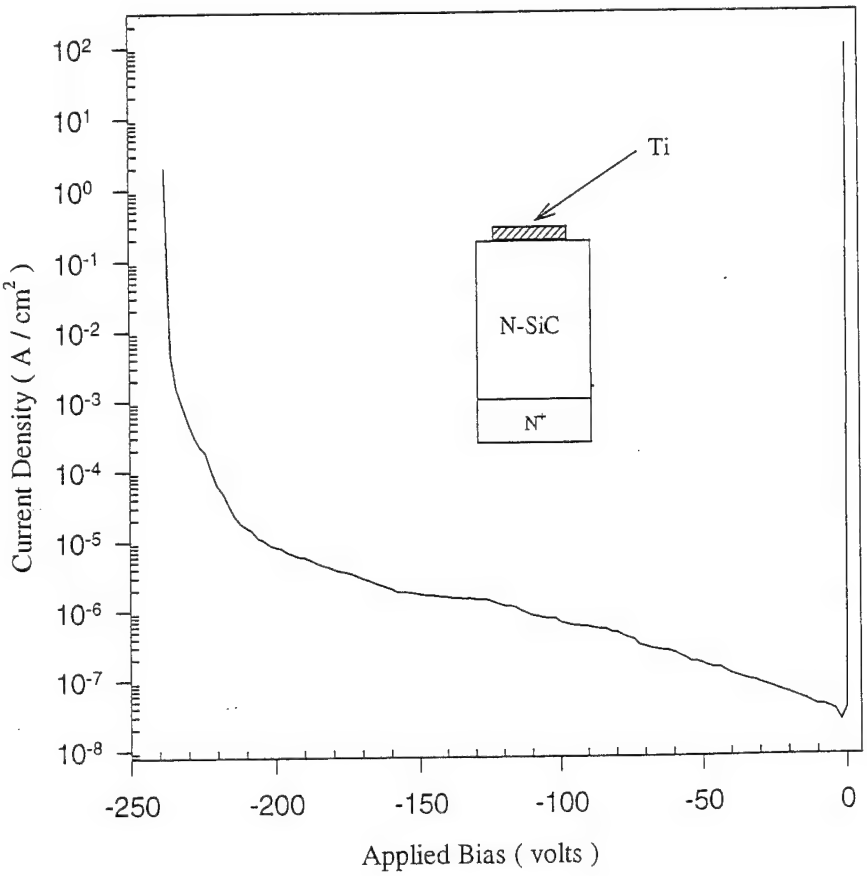


Fig. 6 : J-V characteristics of the Schottky diode test element. The breakdown for the unterminated structure is ~ 240 V

C. Conclusions and Future work

In conclusion, the simulations and experimental work performed in this research indicate that the HJFET is an excellent FET structure to utilize the advantages offered by SiC over silicon. The process for fabrication of the HJFET is fairly simple and does not involve any critical alignments. The operation of the HJFET depends on the ability of P^+-polysilicon /N-SiC heterojunction to block large voltages with a low leakage current. It is also important to be able to etch trenches with smooth side-walls and trench bottom.

However, the fabricated P^+-polysilicon / N-SiC heterojunction was found to have poor reverse I-V characteristics. The heterojunction was formed by depositing polysilicon in a trench etched in SiC. As discussed in section IV, the trenches etched in SiC were rough at the bottom. This results in a bad interface at the P^+-polysilicon / N-SiC junction giving rise to high leakage currents. It is important to standardize the RIE process for etching trenches in SiC so that trenches with smooth features can be obtained. The properties of the P^+-polysilicon / N-SiC heterojunction need to be carefully studied.

Poor step coverage by photoresist of the polysilicon pad at the fifth mask level resulted in gate to source shorts, severely hampering the performance of the HJFET. This problem could be avoided by subjecting the polysilicon to an unmasked etch, prior to a masked etch at the fourth mask level, so as to obtain a step of only 1 to1.5 μm, which could be easily covered, rather than a 4 μm step. Alternately, the sixth-mask level (for the metal patterning) could be redesigned such that the source metal does not run around the polysilicon pad thus, eliminating any possibility of gate to source shorts. However in this case an alternate edge termination would have to be designed for the polysilicon pad.

References:

[1] J. W. Palmour, J.A. Edmonds, H. S. Kong, and C. H. Carter, "Silicon carbide power devices," *Inst. Phys. Conf.,* 1994, ser. 137, ch. 7, pp. 645-655, 1993.

[2] B. Jayant Baliga, " Modern Power Devices," Wiley Inter-science Publication, 1987.

[3] D. Alok, B. J. Baliga and P. K. McLarty, "A simple edge termination for silicon carbide devices with nearly ideal breakdown voltage," *IEEE Electron Device Lett.*, vol. 15, pp. 394-395, 1994.

VI. GROWTH VIA CHEMICAL VAPOR DEPOSITION AND CHARACTERIZATION OF 6H- AND 4H-SiC AND AlN THIN FILMS

Abstract:

A system has been fabricated for the chemical vapor deposition of 4H- and 6H-SiC thin films. The unique design incorporates a separate load lock from which the growth chamber and a reflection high energy electron diffraction (RHEED) chamber are attached. Most of the system hardware has been assembled. Electrical wiring and gas line assembly has been completed to the extent possible. Required electrical and water connection requirements have been requested and are being designed at this time. All power supply components have been received. Recently implemented safety concerns have resulted in the current retrofitting of newly assigned laboratory space to address these issues.

A. Experimental Procedures

The system design is comprised of a six way cross, serving as a loadlock, from which growth and RHEED chambers will be attached. Schematics of the system and the gas panel assembly are shown in Figures 1 and 2. Both chambers are perpendicular to the axis of the loadlock. The sample will be transferred to and from the various chambers on a SiC coated graphite susceptor platform on which the sample will be placed. The transfer mechanism consists of a platform which is moved from chamber-to-chamber by means of a manipulator rod and which is screwed to the side of the susceptor.

The growth chamber consists of a rotating module to which the susceptor is attached. Film growth will be achieved with the sample inverted, i. e., with gases flowing upward while the susceptor is being rotated. The susceptor is attached to the rotating rod assembly by a groove into which the susceptor slides when transfer of the sample occurs. Once the sample is transferred to the rotating rod, the latter is moved down to the quartz portion of the reaction chamber. The sample will be inductively heated via RF coil, and gases introduced from the bottom of the reactor. The growth temperature will be monitored by an optical pyrometer mounted outside the quartz chamber and aimed at the sample. Growth processes, such as gas flow rate and pressure, will be monitored by electronic sensors. Gas flow will be controlled by mass flow controllers and pressure by capacitance manometers.

The RHEED chamber will be employed to monitor film crystallinity, crystal structure and the formation of new surfaces. Since the growth of high quality crystalline SiC films

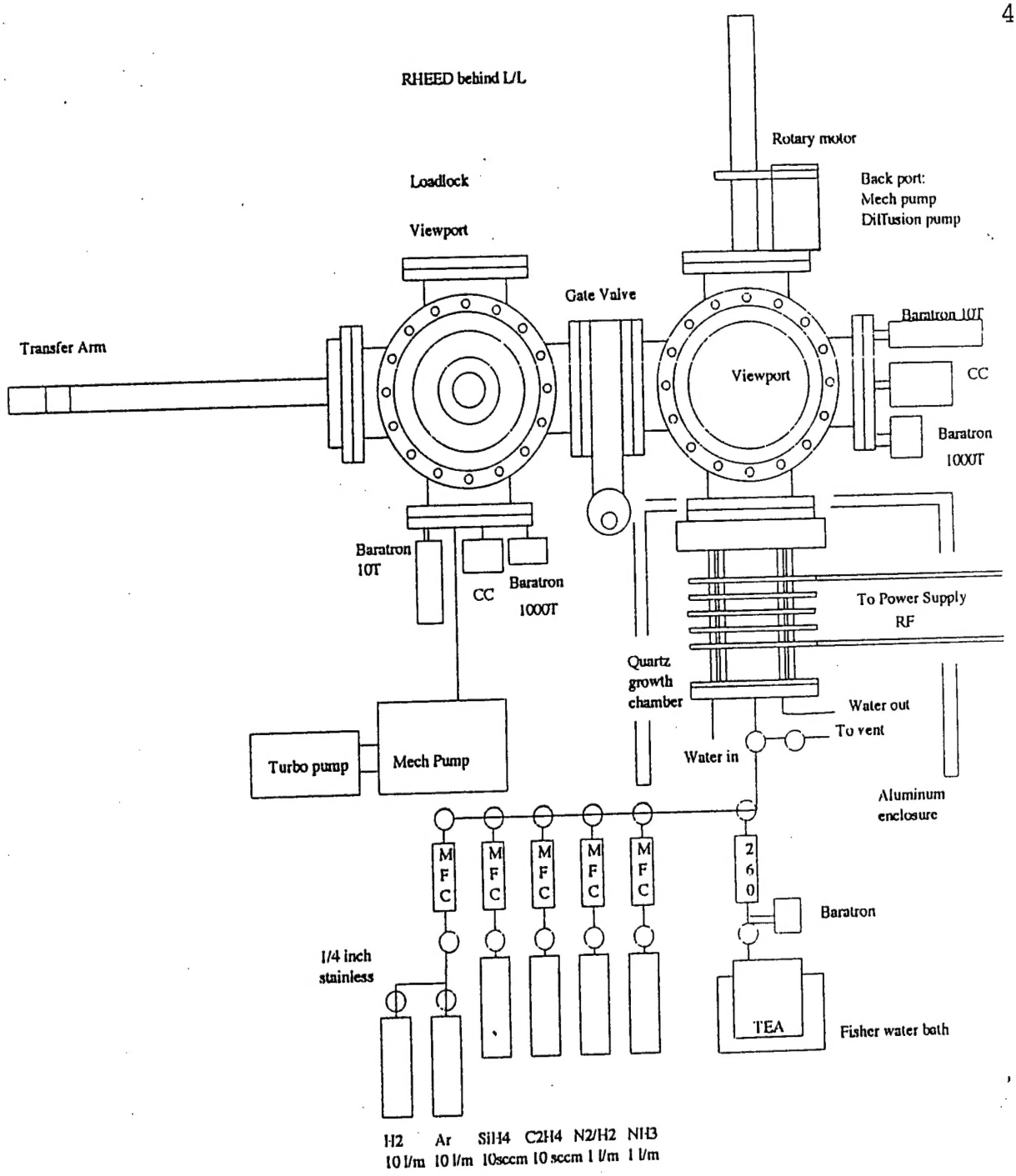


Figure 1. Schematic of AiC CVD growth system: Loadlock and growth chamber side view.

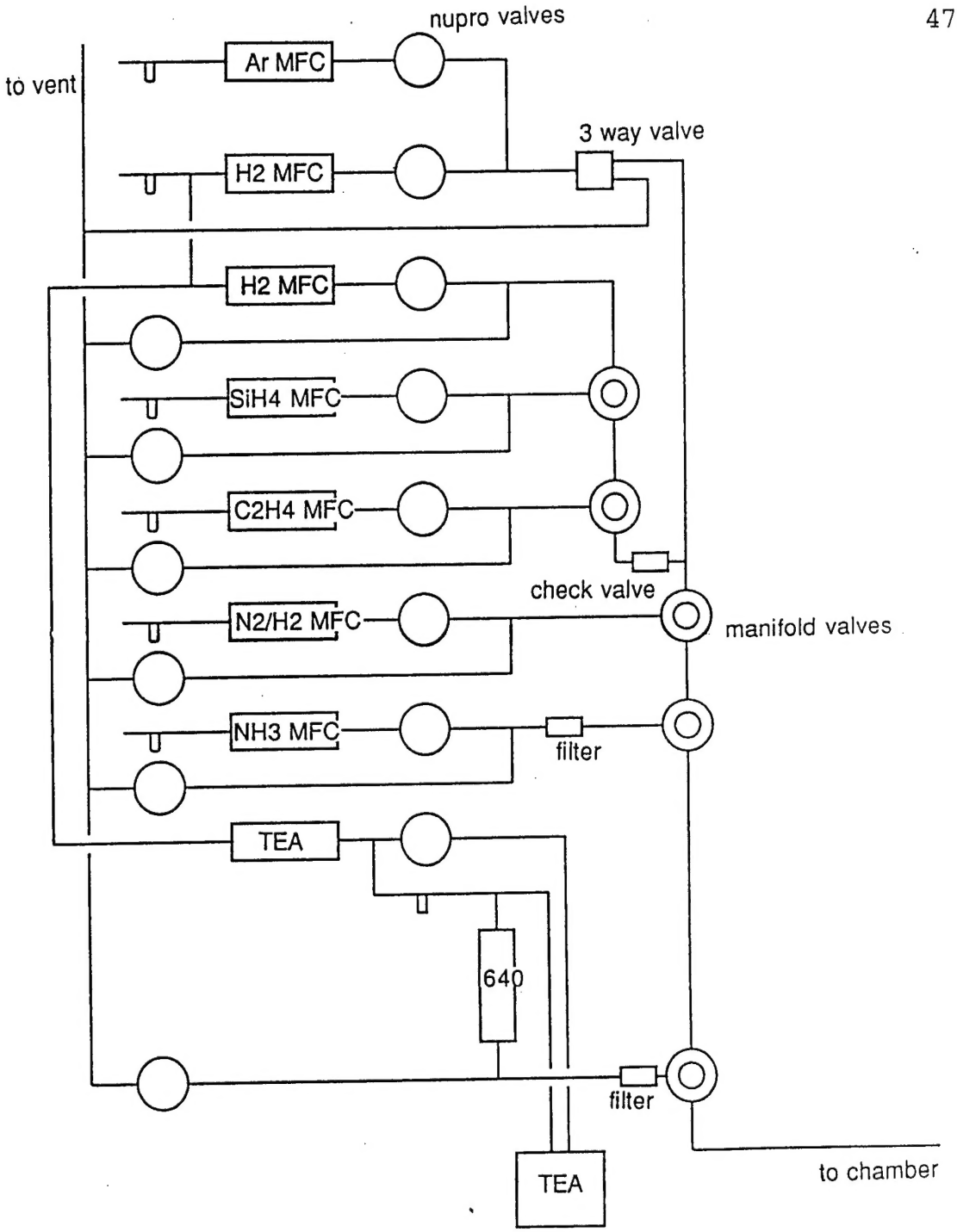


Figure 2. Gas panel assembly.

is the primary goal, a RHEED chamber which is attached to a nominal high vacuum to prevent direct exposure to atmosphere after growth will be useful to characterize the surface structure of the films.

The SiC growth process will employ SiH_4 and C_2H_4 as the reactive components carried in a H_2 diluent. Nominal flow rates will be on the order of 1 to 10 sccm for each reactant. Flow rates of H_2 will be on the order of 3 liters per minute. Other gases which will be included on the system will be NH_3 and an N_2/H_2 mixture for doping and Ar. Triethylaluminum will also be used for doping and maintained at a constant temperature by a heater bath.

The process procedure will include ramping to the SiC growth temperature between 1600-1700°C. Once the temperature is stabilized, the H_2 carrier gas will be introduced followed by the SiC precursor gases. The deposition rate will be determined to produce films of superior quality.

B. Scope of Research

The initial and primary research effort upon completion of the system construction and installation will be the growth of 4H and 6H-SiC homoepitaxial films with a minimum of line and planar defects and unintentionally added impurities. These films will be grown via the optimization of growth conditions including total and partial pressures, gas flow rate, gas flow rate ratios and temperature. The characterization of these defects and impurities by TEM microstructural and SIMS analyses, respectively, and the identification of their origin will be a second important thrust of this research.

C. Results

To date, the following has been accomplished:

1. Stainless steel chambers for sample transfer, growth, and RHEED analysis have been designed and fabricated for the system.
2. Three six-way crosses have been joined with the associated gate valves on the frame, and available flanges and window ports have been attached.
3. A quartz chamber-to-cross assembly has been machined which will provide a sealed interface between two parts of the growth chamber.
4. Quartz cylinders have been cut to the design dimensions
5. Flange parts, pressure gauge attachments, pump connection parts and a rotating rod assembly have been machined.
6. An RF generator has been refurbished and delivered, and will be used to provide RF heating to the susceptor.
7. The assembly of a switch panel to control the gas valves and to enable computer control has been completed
8. A RHEED chamber manipulator has being fitted with a holder to accommodate the susceptor upon transfer
9. Electrical wiring of the switch panel to control the gas flow valves has been

assembled

10. Various gas lines have been assembled on a panel
11. Installation of electrical and water lines for the system as well as safety changes in the laboratory have been requested.

D. Discussion

The proposed design was developed with many sources of input. A number of constraints determined the design configuration and materials used in the system.

One of the main concerns was the high operating temperature of the growth chamber. Since temperatures of 1600-1700°C will be used to grow the SiC films, it was determined that quartz would be the best material for the growth portion of the chamber. A design was subsequently developed to cool the chamber. A double-walled quartz vessel, water cooled around the perimeter, was determined to be the optimum mode of cooling.

Another concern was the transfer mechanism of the susceptor and the placement of samples on the susceptor surface. It was decided that small Ta clips would be the most flexible for our purposes to accommodate various sized samples. For the transfer mechanism, a simple tongue-in-groove assembly, moved between chambers by means of a transfer arm which would screw into the side of the susceptor, was deemed simplest and most practical.

E. Conclusions/Future Research Plans and Goals

A system design to deposit SiC thin films has been developed. Most components have been either received or are in transit. Other needed parts are currently being machined. Further assembly of the system is expected when electrical and water sources to the building enable us to start up many parts of the system.